Preliminary Data Sheet

MS1135

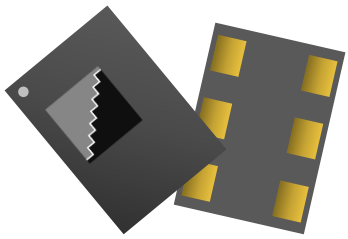
Ultra-Low Phase Jitter Digitally Synthesized Oscillators (DSO)

Features

- Factory Programmable
  - Any frequency from 10 MHz to 1000 MHz
  - Differential Output: CML/LVDS/LVPECL/LVDS-EXT/HCSL
- Ultra-Low RMS phase jitter (12 KHz to 20 MHz)
  - 35 fs at 156.25 MHz
  - 25 fs at 312.50 MHz
  - 26 fs at 491.52 MHz
  - 27 fs at 625 MHz
- Total stability of ±20 ppm
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Standard 2.5X2.0 mm 6-pin LGA package
- 2.5V/3.3V supply with internal regulator
- Superior power supply immunity
- Industrial Temperature range: -40°C to 85°C
- Extended Temperature range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- Network Equipment (Optical Modules, routers)
- 100G/200G/400G/800G/1.6T/3.2T OTN, Coherent optics
- Storage, switches, servers, NICs, accelerators
- 3G to 24G SDI broadcast video
- 10G/40G/100G optical ethernet
- 112G/224G/448G PAM4 Clocking
- Test and measurement equipment



General Description

The MS1135 is a digitally synthesized oscillator (DSO) that combines advanced Bulk Acoustic Wave (BAW) resonator technology with high-performance digital frequency synthesis to deliver highly stable, fully programmable multi-GHz clocks with extremely low phase Jitter.

Built-in Adaptive Intelligence continuously monitors operating conditions in the background, using autonomous DSP algorithms to maintain robust and consistent performance across process, voltage, and temperature.

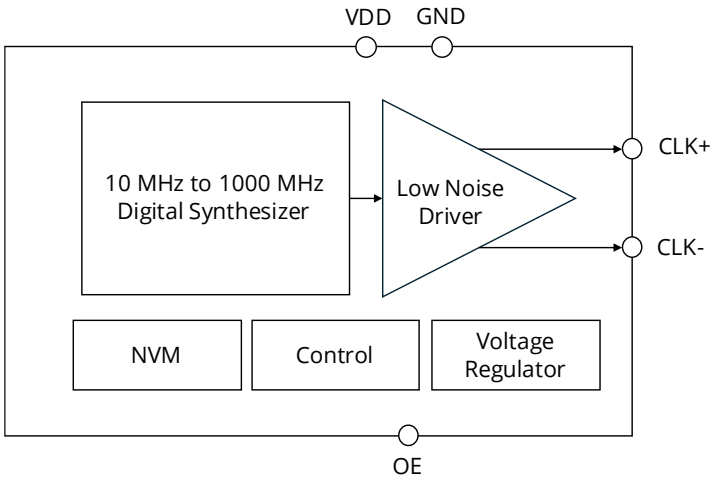
The devices are factory programmed to provide an accurate frequency between 10 MHz and 1000 MHz at less than 1 ppb resolution.

The MS1135 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

Device Information

Part Number	Package	Description
MS1135	2.5x2.0 mm 6-pin LGA	Oscillator

Figure 1. Functional Block Diagram



MS1135

Pin Assignment and Pin Description (TOP VIEW)

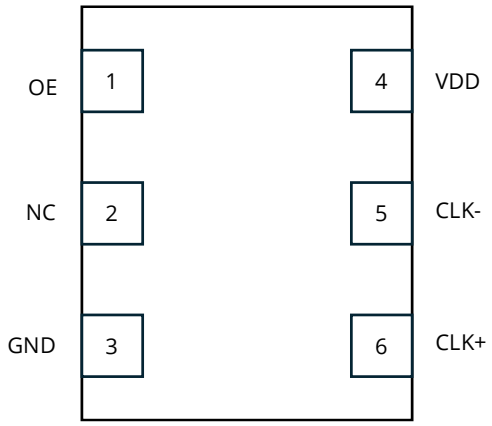


Figure 2. MS1135 Pin Assignments

Table 1. MS1135 Pin Descriptions

Pin No	Name	Description
1	OE	Output Enable • High/Floating: Output enabled (Internal pull-up of 100kΩ) • Low: Output disabled
2	NC	No Connect – leave floating
3	GND	Ground
4	CLK+	True Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply – connect bypass capacitor between this pin and pin 3. Keep bypass as close as possible to the pins

Part Ordering Information

Figure 3 shows a logic tree for ordering each of the available parts.

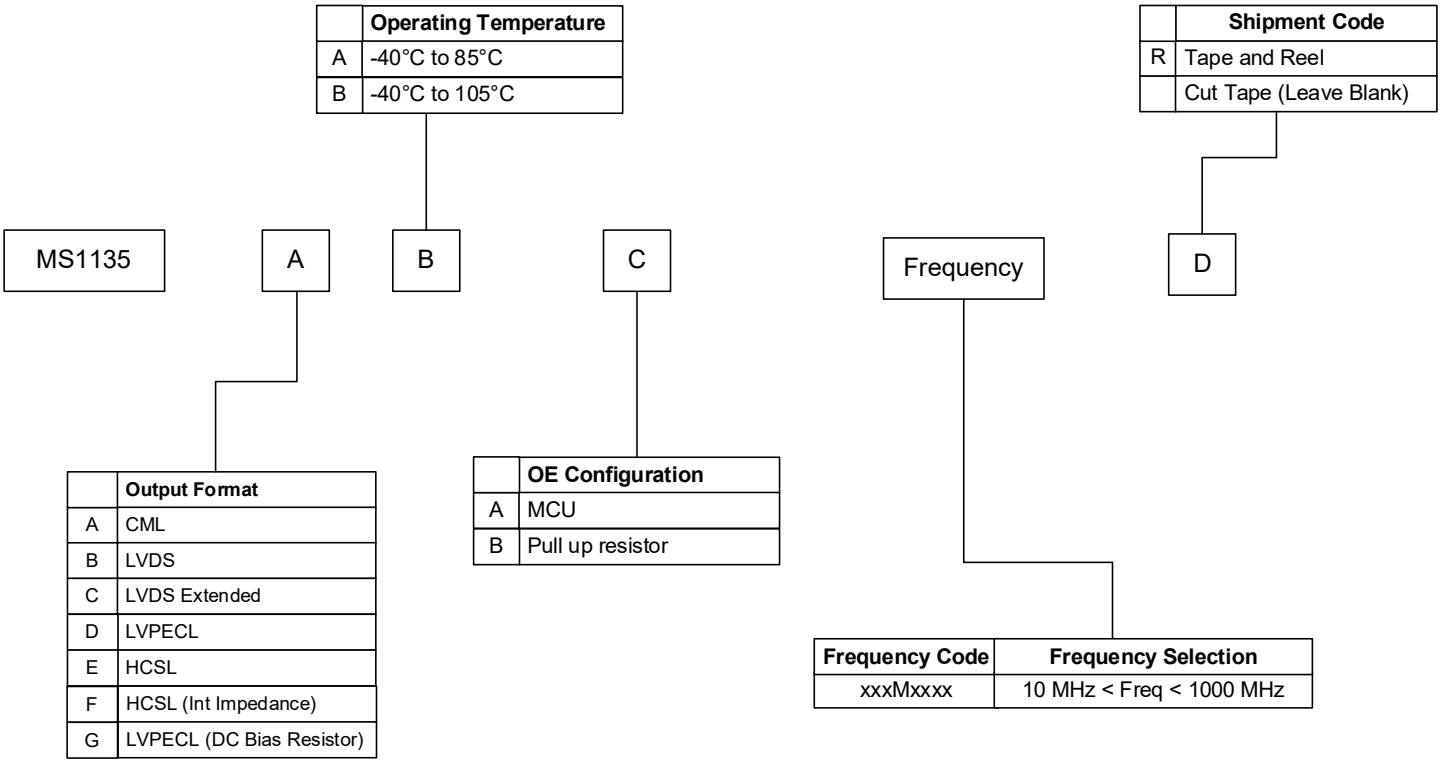


Figure 3. MS1135 Part Ordering Information

Table 2. Example of ordering part number

Base P/N	Output Format	Operating Temperature	OE Configuration	Frequency Code	Shipment Type	**Ordering part number**
MS1135	LVDS	-40°C to 85°C	MCU	312.5 MHz	Tape and Reel	**MS1135BAA312M5000R**
MS1135	LVPECL	-40°C to 105°C	Pull up resistor	625 MHz	Tape and Reel	**MS1135DBB625M0000R**

Specifications

Table 3. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=2.5/3.3V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard output terminations (See Figure 9-15). A 0.1uF and 10uF bypass capacitors should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Frequency Range	F_{CLK}	All Output Formats	10		1000	MHz
Frequency Stability						
Frequency Stability*	F_{STB}		-20		20	PPM
*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year, +25°C). Aging is estimated from environmental reliability tests;						
Clock Output Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz integration band)	Φ_{JITTER}	Frequency=312.5 MHz		25	37	fs
		Frequency=625 MHz		27	40	fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		2.375		3.465	V
Temperature Range	T_A	Industrial Temperature	-40	25	85	°C
		Extended Industrial Temperature	-40	25	105	°C

Current Consumption

Supply Current Consumption	I_{DD}	LVDS Output (Output Enabled)		80	100	mA
		All Other Outputs (Output Enabled)		90	110	mA
		Tristate Hi-Z (Output Disabled. OE=0)		50	60	mA

Input Characteristics

Digital Input Levels(OE)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10 Char data	ms

PSRR Characteristics

Center Frequency= 312.5 MHz		
Ripple Frequency (50mVpp)	Power Supply-Induced Phase Noise Spur (dBc)	Power Supply Induced Jitter Sensitivity (fs/mV) Peak-to-Peak
1 KHz	-105	< 0.1
5 KHz	-125	< 0.1
10 KHz	-133	< 0.1
50 KHz	-150	< 0.1
100 KHz	-155	< 0.1
1 MHz	-161	< 0.1
10 MHz	-164	< 0.1

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		50	70	ps
CML Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 9, Figure 10	0.6	0.8	1	V
LVDS Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 11	0.5	0.7	0.9	V
LVDS-EXT Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 11	0.8	1.2	1.6	V
LVPECL Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 12, Figure 13	1.2	1.4	1.6	V
HCSL Output (AC or DC-Coupled)	Vpp	Differential Pk-Pk See Figure 14, Figure 15	1.1	1.35	1.6	V
Overshoot Voltage, peak (All output types)	Vos	Measured as a percentage of differential swing Vpp		6		%
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

Unless otherwise specified, all differential output amplitudes are measured across a 100 Ω differential load or the termination network shown in the referenced output driver figures on the following pages

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit
Supply Voltage	-0.3	3.465	V
Digital I/O (OE)	-0.3	3.465	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Junction Temperature		150	°C
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

Table 5. Environmental Compliance

Parameter	Test Condition	Value	Unit
Moisture Sensitivity Level (MSL)	MSL3 @260°C		
Soldering Temperature	MIL-STD-883, Method 2003	260	°C
Electrostatic Discharge (HBM)	JEDEC JS-001	2000	V
Charge-Device Model (CDM)	JEDEC JESD22-C101	500	V
Latch-up Compliance	JESD78 Compliant		

Table 6. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
2.5mm x 2mm 6 pin LGA	Maximum Board Temperature	T_B	125	°C
	Thermal Resistance, Junction to Ambient	$ø_{JA}$	90	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C
Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

Table 7. Typical Output Phase Noise Characteristics
VDD= 2.5/3.3V, T_A = 25°C, Output Type = LVDS-EXT

Offset frequency	156.25 MHz	312.50 MHz	491.52 MHz	625 MHz	Unit
1 KHz	-106	-103	-100	-98	dBc/Hz
10 KHz	-138	-133	-128	-127	dBc/Hz
100 KHz	-157	-154	-149	-147	dBc/Hz
1 MHz	-167	-163	-158	-156	dBc/Hz
10 MHz	-168	-164	-160	-148	dBc/Hz
20 MHz	-168	-164	-159	-158	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	35	25	26	27	fs

Typical Output Measured Phase Noise Plots

This section shows MS1135 performance plots.

Measurement parameters are: VDD = 2.5/3.3V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent E5052B Signal Source Analyzer.

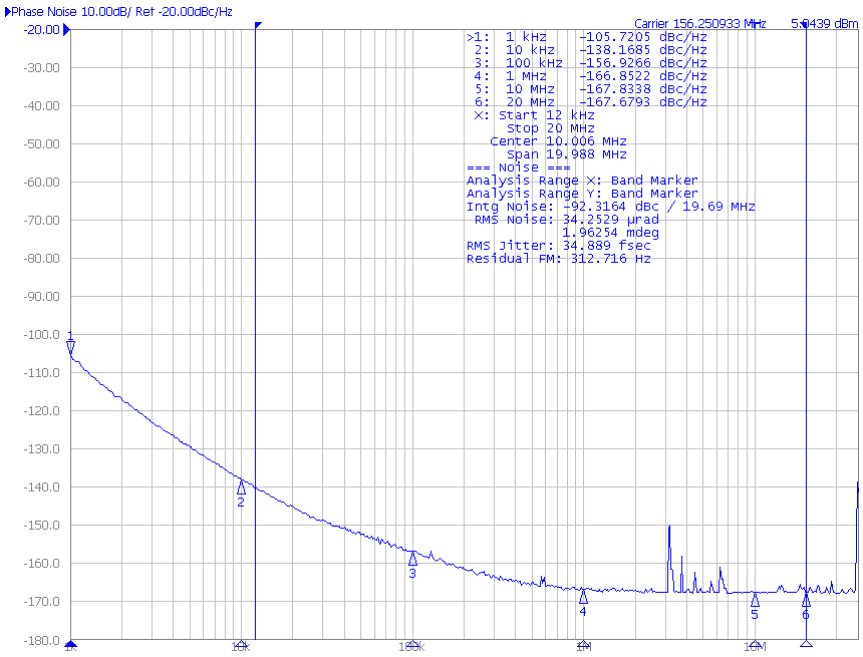


Figure 4. Center Frequency: 156.25 MHz

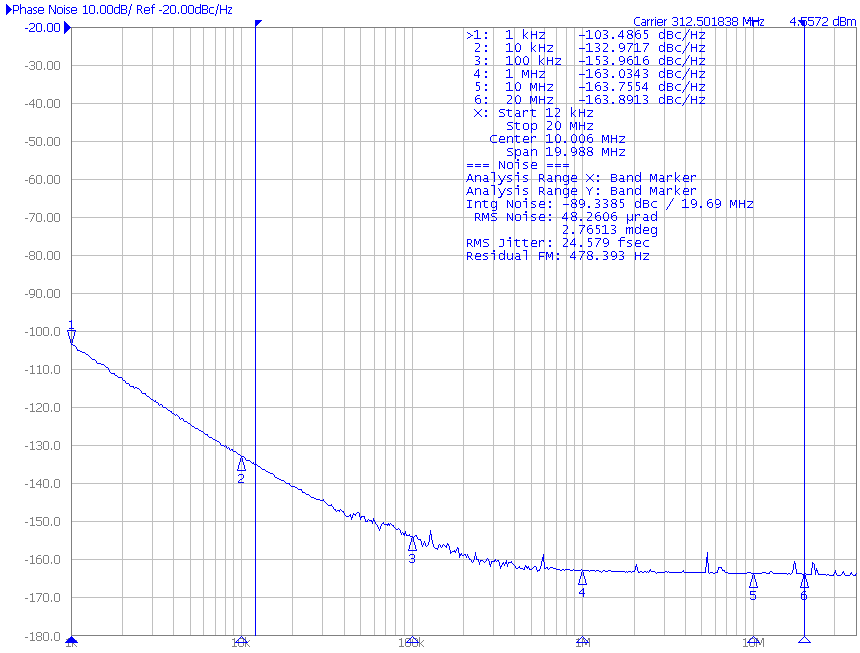


Figure 5. Center Frequency: 312.5 MHz

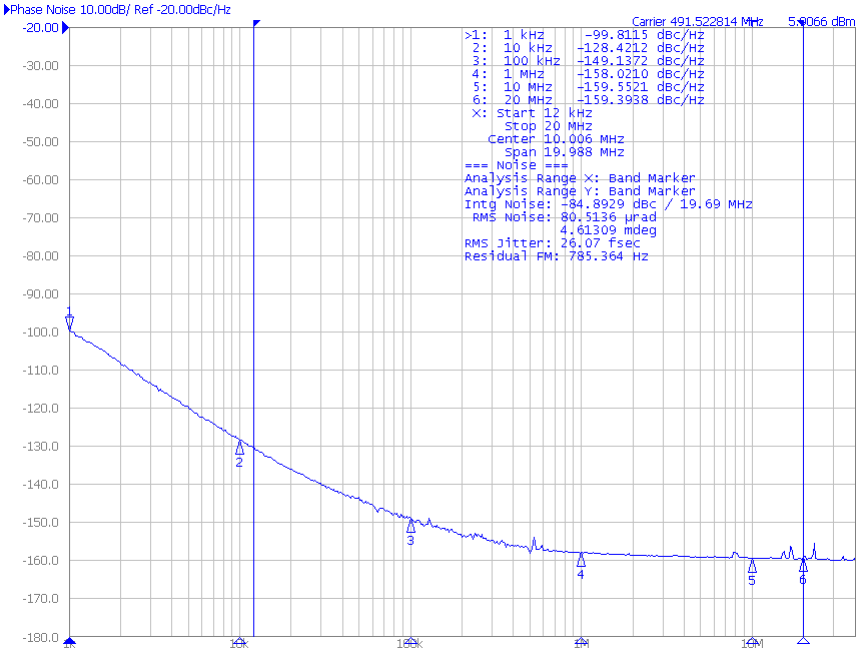


Figure 6. Center Frequency: 491.52 MHz

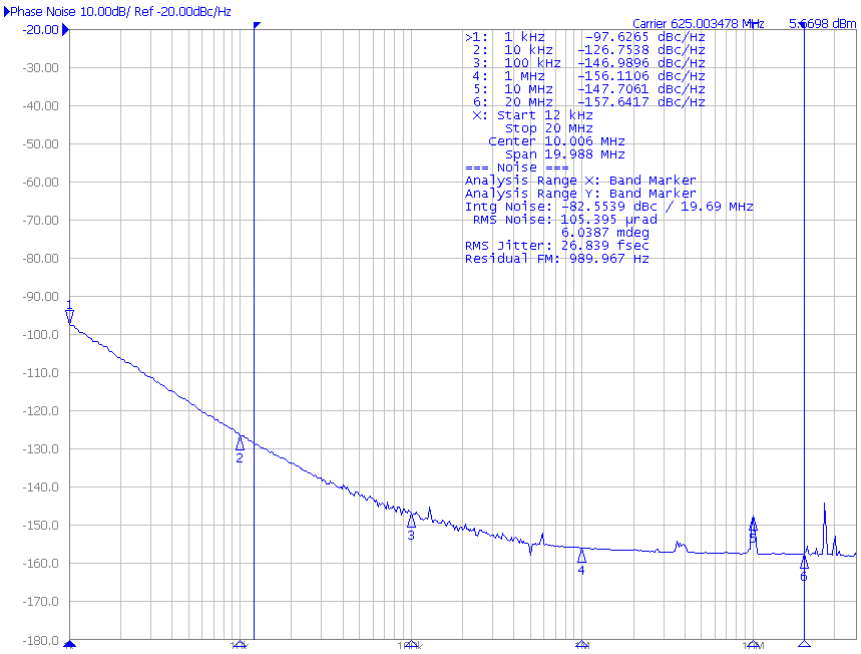


Figure 7. Center Frequency: 625 MHz

Output Terminations

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff
LVDS	0.7V	AC	100 Ω diff
LVDS-EXT	1.2V	AC	100 Ω diff
LVPECL	1.4V	AC	50 Ω to VT
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT
HCSL (Int Term)	1.35V	AC or DC	None

HCSL	1.35V	DC	50 Ω to GND

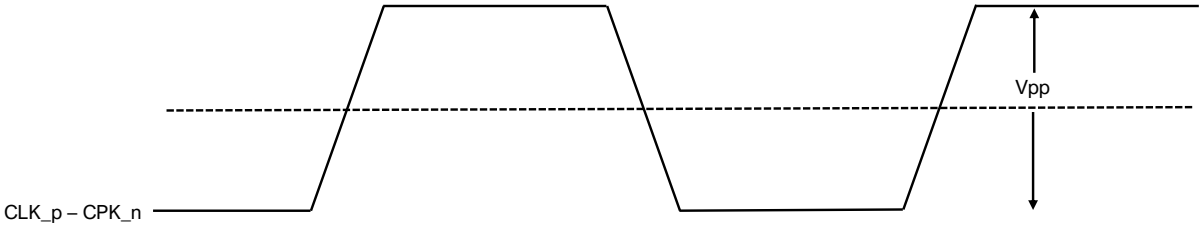


Figure 8. Differential Output Swing

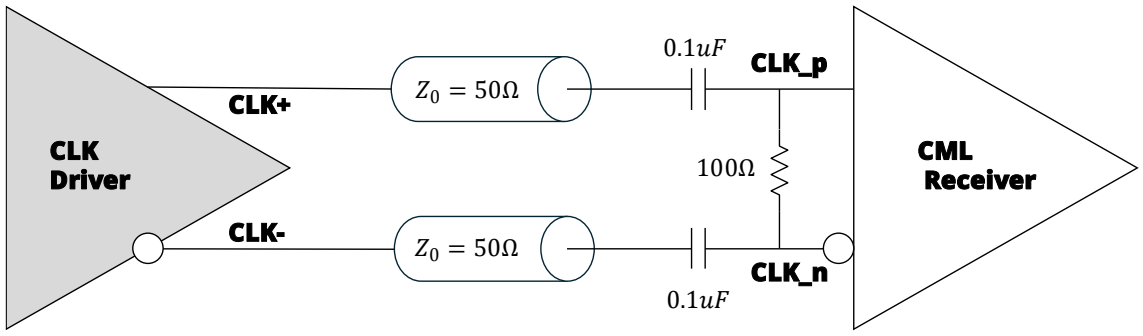


Figure 9. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

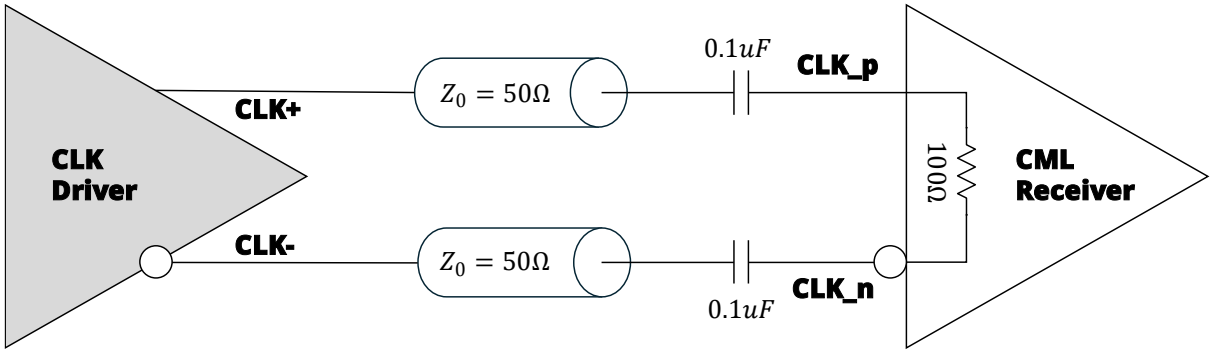


Figure 10. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

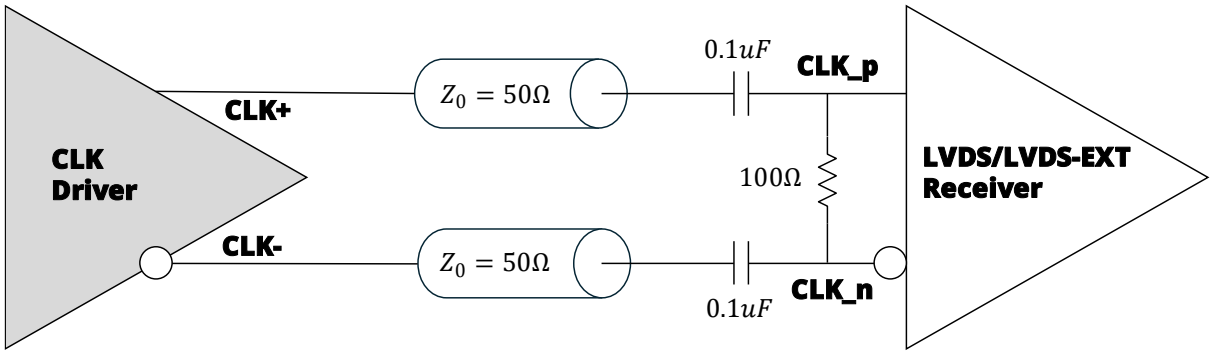


Figure 11. LVDS/LVDS-EXT Output Driver with 100 Ω Differential Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVDS/LVDS-EXT	0.7V/1.2V	AC	100 Ω diff

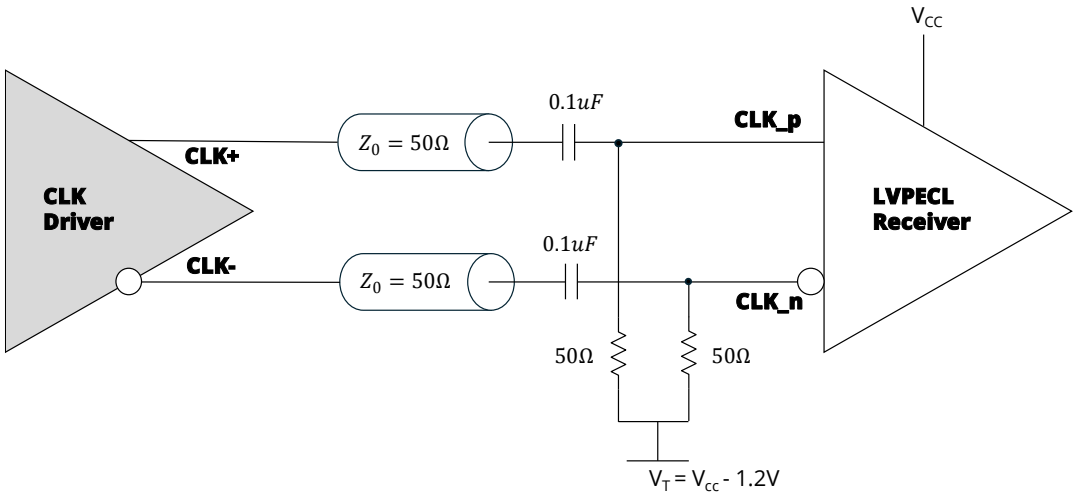


Figure 12. LVPECL Output Driver with External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL	1.4V	AC	50Ω to VT

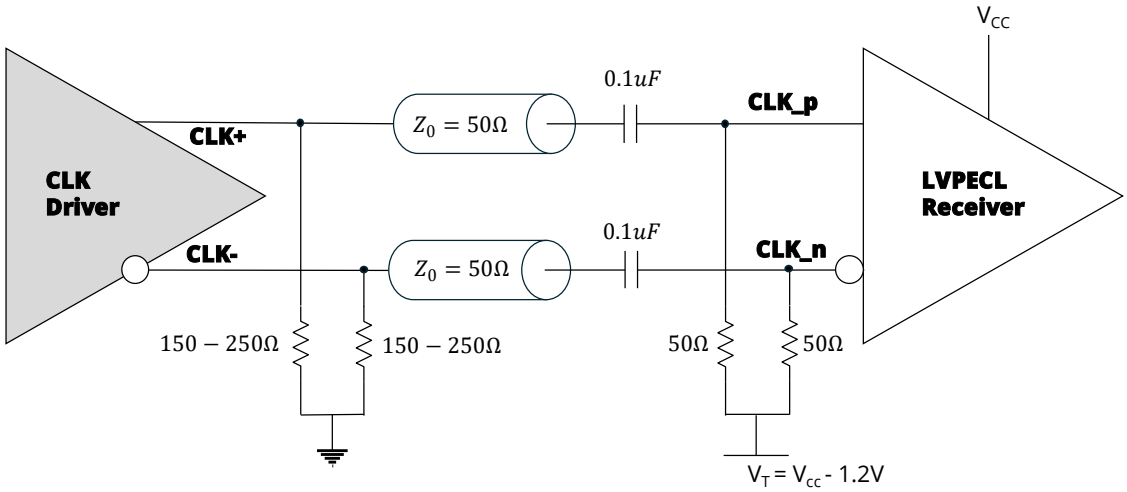


Figure 13. LVPECL Output Driver with Source Bias Resistors and External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT

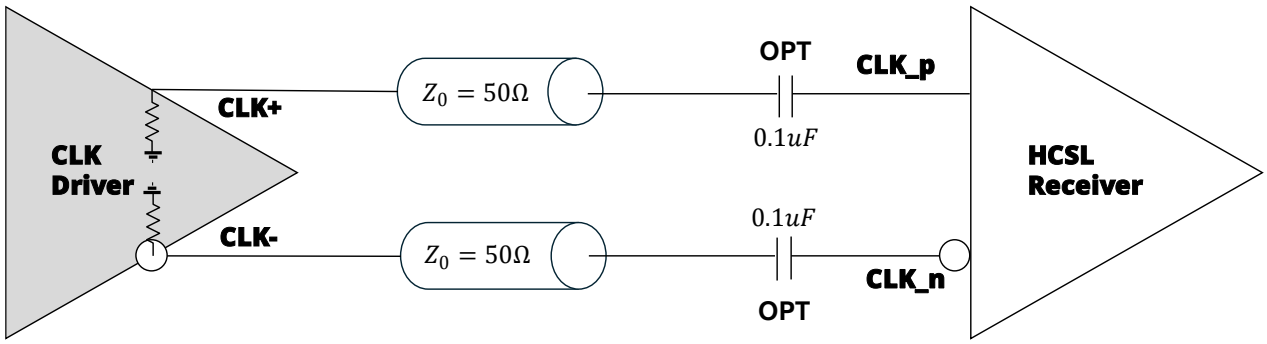


Figure 14. HCSL Output Driver with Integrated Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL (Int Term)	1.35V	AC/DC	None

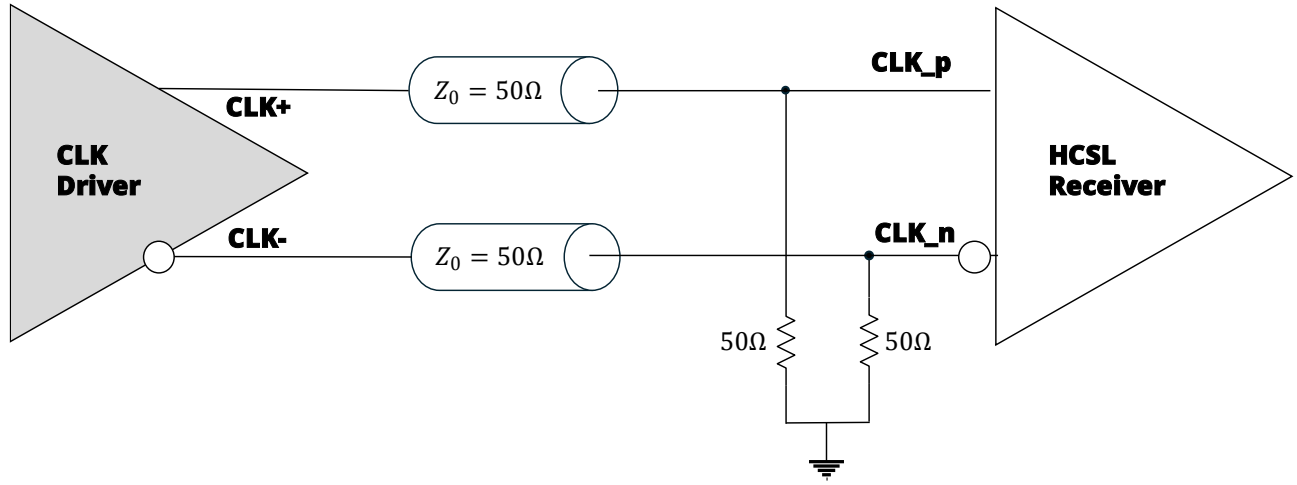


Figure 15. HCSL Output Driver with 50 Ω Receiver Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination

HCSL	1.35V	DC	50 Ω to GND

Output Timing

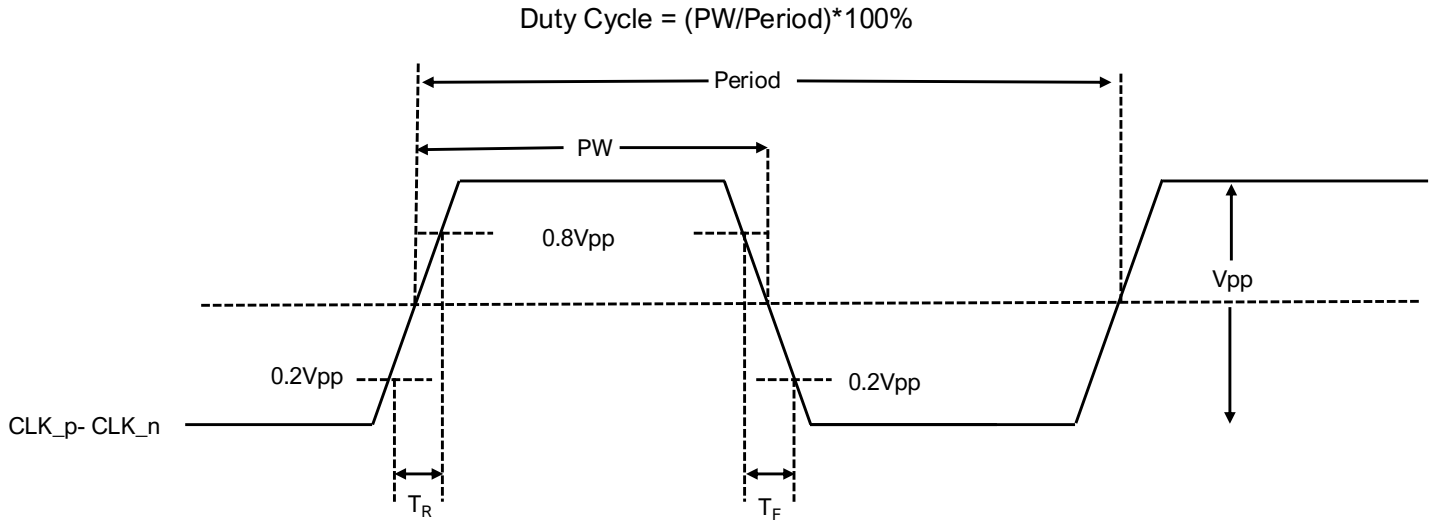


Figure 16. Output Timing across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps

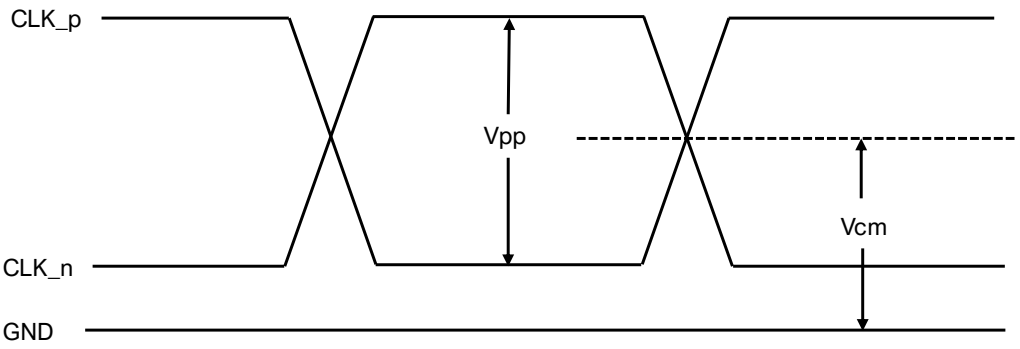


Figure 17. HCSL Output Level across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

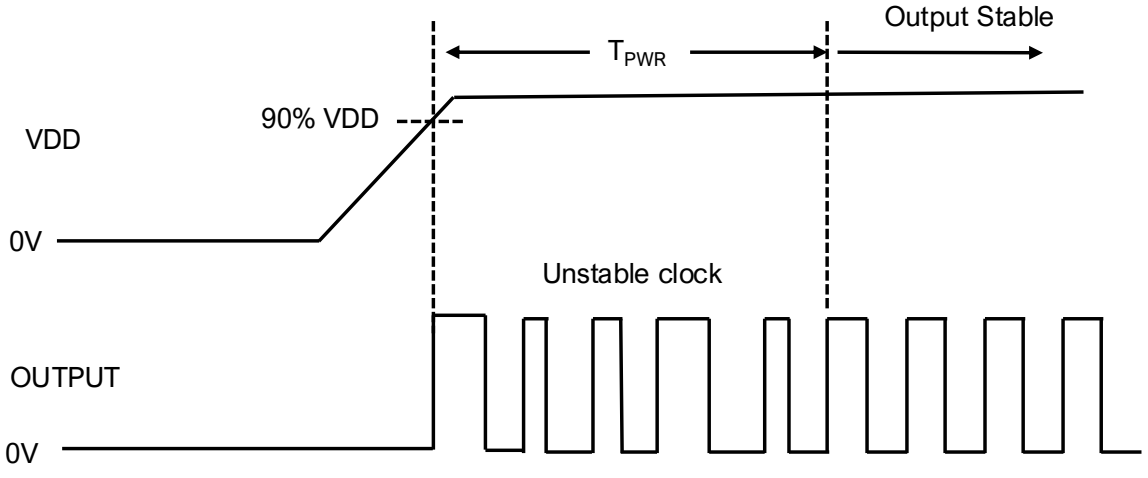


Figure 18. Powerup Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit

Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

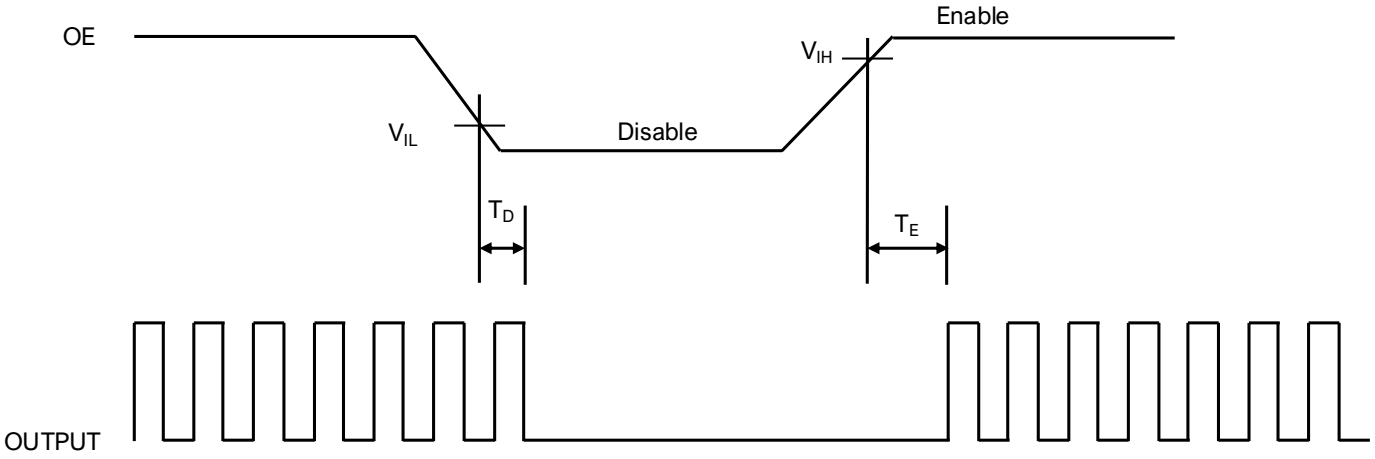


Figure 19. OE Enable/Disable Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs

OE Configurations

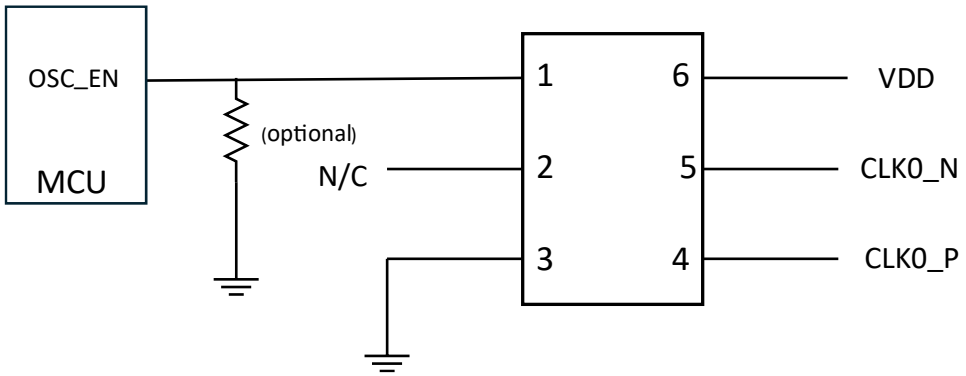


Figure 20. OE Connected to MCU (Optional pull-down resistor)

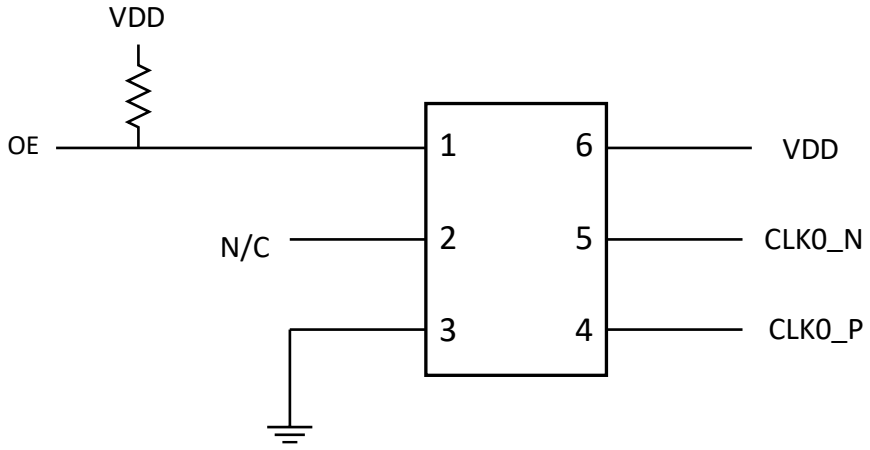


Figure 21. OE Connected to VDD using pull-up resistor

Packaging Information

Figure 22 shows the MS1135 packaging drawing

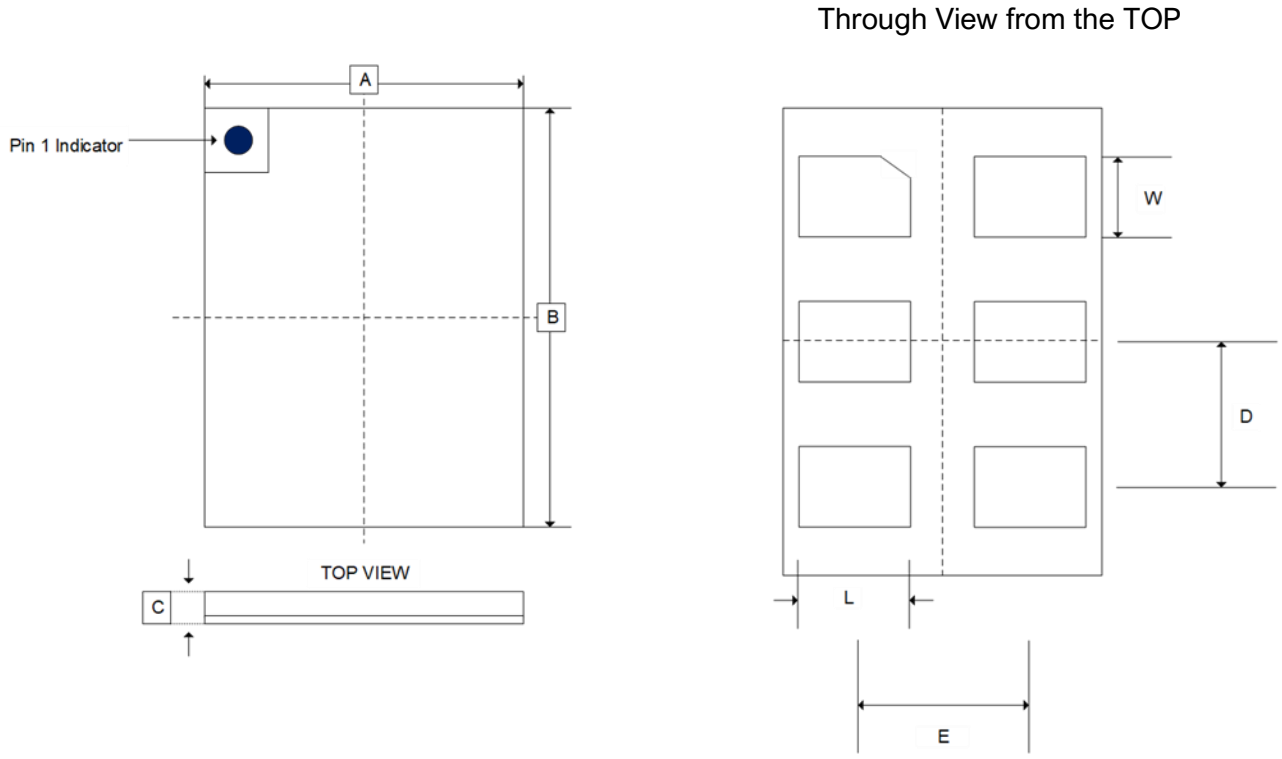


Figure 22. MS1135 Packaging Drawing (2.5X2.0 mm)

Table 8. MS1135 Packaging Dimensions

Dimensions	Min	Nom	Max
A		2.00 BSC	
B		2.50 BSC	
C	1.246	1.346	1.446
L	0.55	0.60	0.65
W	0.35	0.40	0.45
D		0.85 BSC	
E		1 BSC	
Package Edge Tolerance		0.1	
Mold Flatness		0.2	
Coplanarity		0.08	

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 23 shows the MS1135 PCB land pattern.
Note: All dimensions are in millimeters

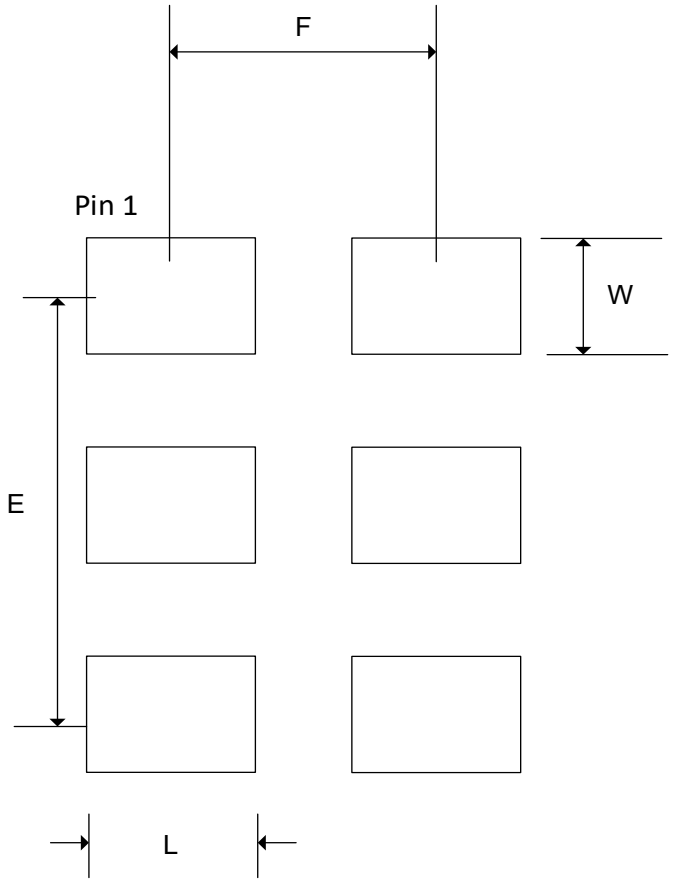


Figure 23. MS1135 Packaging Land Pattern Drawing (2.5X2.0 mm)

Table 9. MS1135 Packaging Land Pattern Dimensions

Dimensions	Length
L	0.75
W	0.55
E	1.7
F	1

Device Top Marking

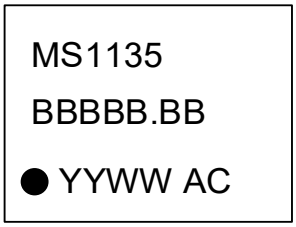


Figure 24. MS1135 Device Top Marking Showing Pin 1

Table 10. MS1135 Device Marking Legend

Line	Position	Description
1	1	Product Marking
2	1-5	Lot Number
	6-7	Wafer Number
3	Lot Trace Code	
	1	Pin 1 Orientation Mark (Dot)
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	7-8	Assembly Code

Reflow Profile (IPC/JEDEC-STD-020)

Figure 25 shows the reflow profile for MS1135

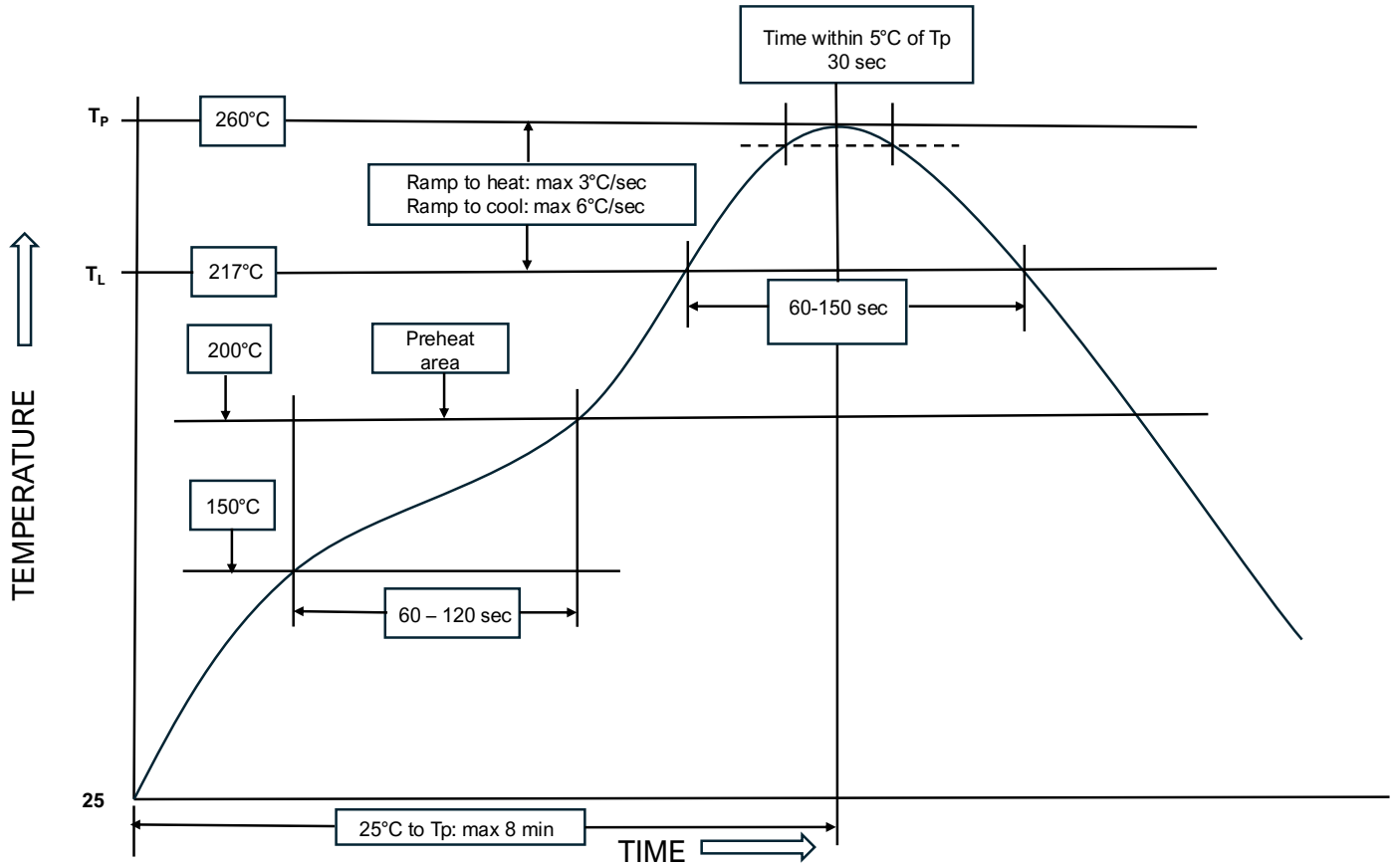


Figure 25. MS1135 Reflow Profile

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