Preliminary Data Sheet

MS2508

High-Performance Jitter Attenuator and Clock Generator

Features

- Input frequency from 1 MHz to 750 MHz, gapped clock
- Output frequency from 20 MHz to 2200 MHz
- Eight programmable outputs
- Programmable integer dividers
  - Divider range: 1 to 64
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 34.9 fs at 156.25 MHz
  - 24.6 fs at 312.50 MHz
  - 26.8 fs at 625 MHz
- Output Formats: LVDS/CML/LVPECL/HCSL/LVDS-EXT
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Industry standard 5X5 mm 40-pin LGA package
- I^2C Interface
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C

Applications

- Datacenter, Switches, Routers, NIC
- High-Speed Networking, 200G-1.6T
- Acceleration / AI, and Compute Nodes
- PCIe Gen.6,nVLink, Ethernet, Optical

General Description

The MS2508 is a low-power, high-performance, fully integrated jitter attenuator and programmable clock generator. It provides eight differential outputs from a single clock domain. It is powered by our Virtual Crystal™ technology that enables ultra stable fully programmable multi-GHz clocks with extremely low phase noise.

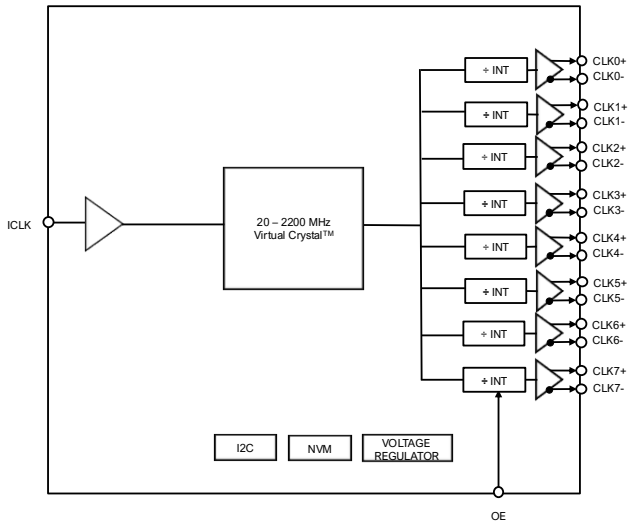
The product can take any input frequency from 1 MHz to 750 MHz and generate any output frequency from 20 MHz to 2200 MHz with <1ppb. The output frequency is synchronized to the input clock.

The product can be factory programmed using non-volatile memory (NVM). This pre-programmed factory setting will be the power up condition of the device for the frequencies and output interface.

Device Information

Part Number	Package	Description
MS2508	5X5 mm 40-pin LGA	JA/Clock Generator

Figure 1. Functional Block Diagram



Pin Assignment and Pin Descriptions

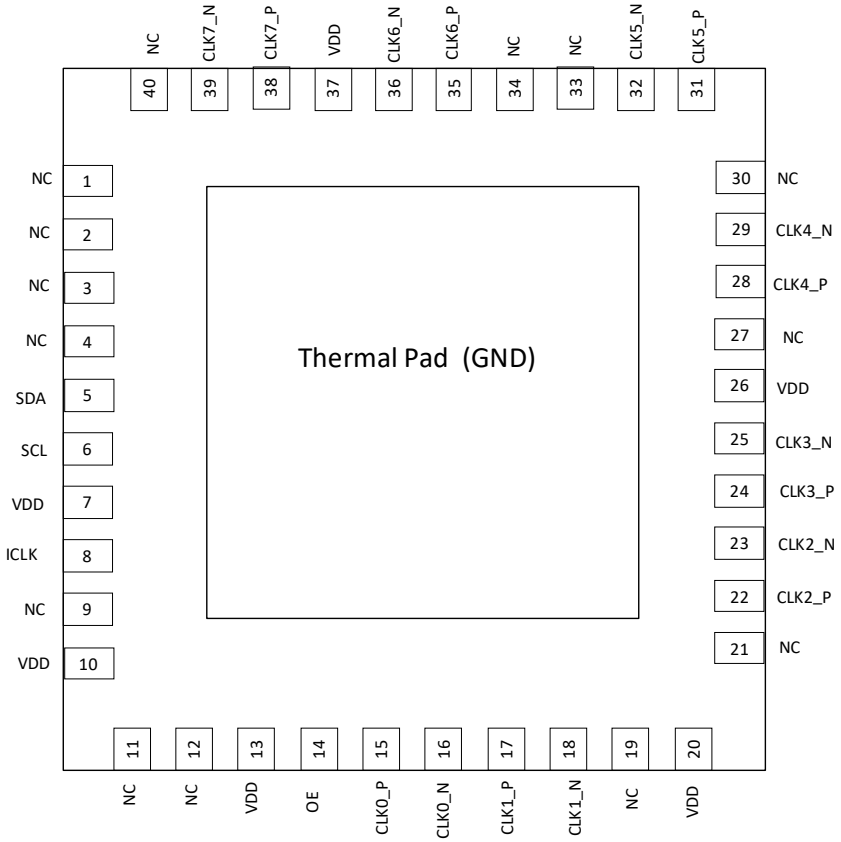


Figure 2. MS2508 Pin Assignments

Table 1. MS2508 Pin Descriptions

Pin No.	Name	I/O	Description
14	OE	I	Output Enable (All outputs)
5	SDA	I/O	I2C Serial Data
6	SCL	I	I2C Serial Clock
8	ICLK	I	Single Ended Input
15	CLK0_P	O	Differential Clock Output
16	CLK0_N		
17	CLK1_P	O	Differential Clock Output
18	CLK1_N		
22	CLK2_P	O	Differential Clock Output
23	CLK2_N		
24	CLK3_P	O	Differential Clock Output
25	CLK3_N		
28	CLK4_P	O	Differential Clock Output
29	CLK4_N		
31	CLK5_P	O	Differential Clock Output
32	CLK5_N		
35	CLK6_P	O	Differential Clock Output
36	CLK6_N		
38	CLK7_P	O	Differential Clock Output
39	CLK7_N		
7,10,13,20,26,37	VDD	POWER	1.8V Power Supply
1,2,3,4,9,11,12,19,21,27,30,33, 34 ,40	NC		No Connect
Thermal Pad (GND)	GND	POWER	Device GND, Thermal Pad

Part Ordering Information

Figure 3 shows a logic tree for ordering each of the available parts.

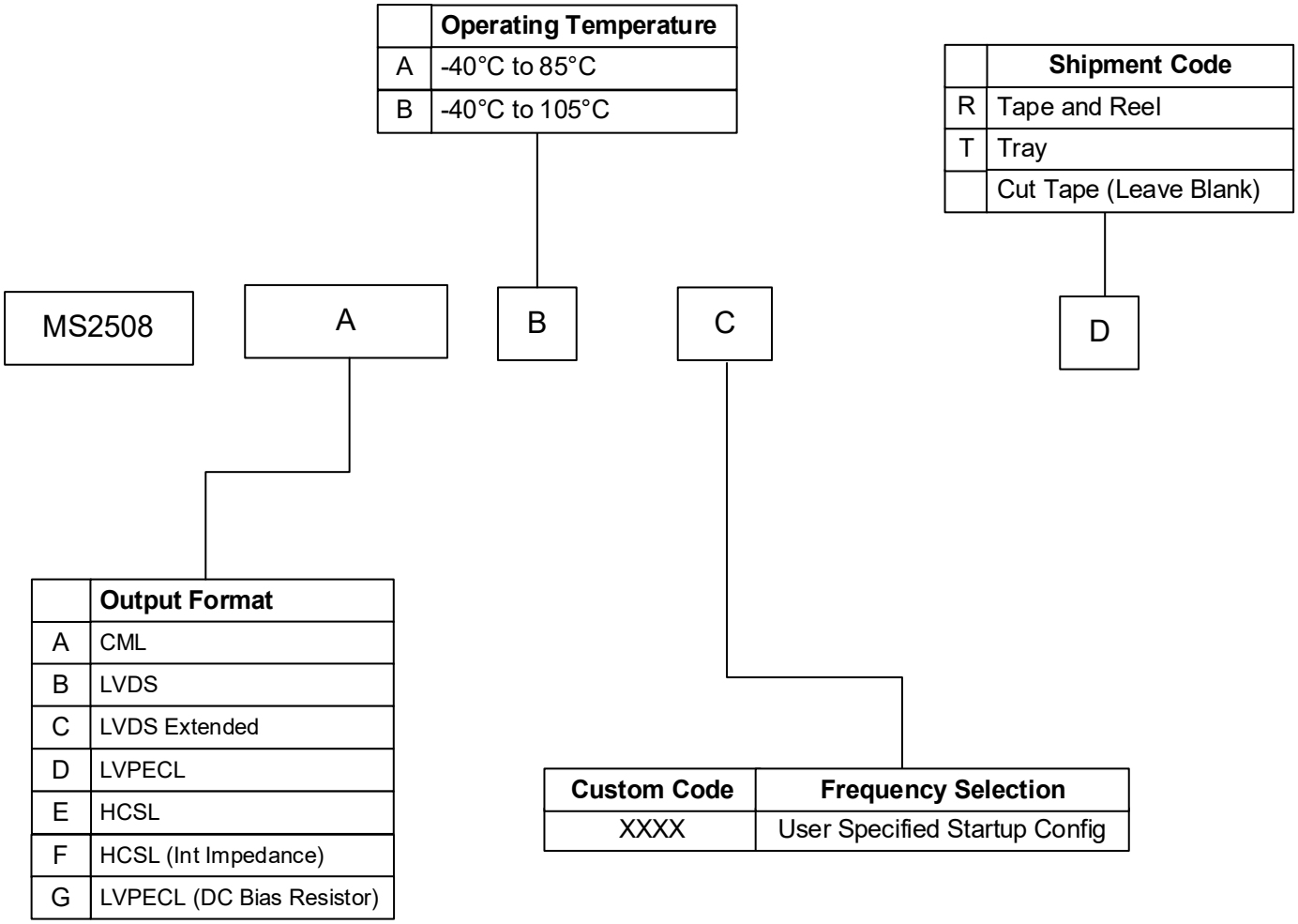


Figure 3. MS2508 Part Ordering Information

Table 2. Example of ordering part number

Base P/N	Output format	Operating Temperature	Frequency Code	Shipment Type	**Ordering part number**
MS2508	LVDS	-40°C to 85°C	0001*	Tape and Reel	**MS2508BA0001R**

* Frequency Code table will be provided by factory based on customer requirements.

Specifications

Table 3. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard output terminations (See Figure 9-15). A 0.1uF and 10uF bypass capacitors should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Input Frequency Range	I_{CLK}		1		750	MHz
Input Voltage Swing	I_{SWG}	AC-coupled	0.1		1.8	Vpp-SE
Output Frequency Range	F_{CLK}	All Output Formats	20		2200	MHz
Frequency Stability						
Frequency Stability*	F_{STB}		-20		20	PPM
*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year, +25°C). Aging is estimated from environmental reliability tests;						
Clock Output Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz integration band)	Φ_{JITTER}	Frequency=491.52 MHz		22	33	fs
		Frequency=625 MHz		20	30	fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		1.71 (-5%)	1.8	1.89 (+5%)	V
Temperature Range	T_A	Industrial Temperature	-40	25	85	°C
		Extended Industrial Temperature	-40	25	105	°C

Current Consumption

Supply Current Consumption	I_{DD}	LVDS Output (Output Enabled)		160	190	mA
		All Other Outputs (Output Enabled)		150	180	mA
		Tristate Hi-Z (Output Disabled. OE=0)		70	84	mA

Input Characteristics

Digital Input Levels(OE/SDA/SCL)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs
Output Lock Time (JA Mode)	T_{LOCK}	Time from input signal to a stable output	10			ms
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (1) (Center Frequency is 312.5MHz)		-110		dBc
Power Supply-Jitter Sensitivity	PSJS			0.2		fs/mV

Note:

(1) Measured with 50 mVpp ripple from 500 KHz to 10 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps
CML Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 12, Figure 13	0.6	0.8	1	V
LVDS Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 14	0.5	0.7	0.9	V
LVDS-EXT Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 14	0.8	1.2	1.6	V
LVPECL Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 15, Figure 16	1.2	1.4	1.6	V
HCSL Output (AC or DC-Coupled)	Vpp	Differential Pk-Pk See Figure 17, Figure 18	1.1	1.35	1.6	V
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV
Output-Output Crosstalk	XTALK	Measure spur from adjacent output		-75		dBc

Unless otherwise specified, all differential output amplitudes are measured across a 100 Ω differential load or the termination network shown in the referenced output driver figures.

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O (OE/SDA/SCL)	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Junction Temperature		150	°C
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

I2C Interface

Table 5. I²C Timing Specifications
VDD=1.8V +/-5%, Ta= Operating Temperature

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Units
SCL Clock Frequency	tFCL			100	400	KHz
Data Set-up Time	tSU		80			ns
Data Hold Time	tHD		0			ns
Data Valid Time, Data Acknowledge Time	tVD		0.85			us
Hold time for START Condition	tHDSTART		0.5			us
Set-up time for STOP Condition	tSUSTOP		0.5			us
Low Period of SCL Clock	tLOW		1.2			us
High Period of SCL Clock	tHIGH		0.5			us
Bus Turnaround Time Between STOP and START Condition	tBUF		2			us
Note: SDA/SCL pins requires 470Ω pull-up resistor						

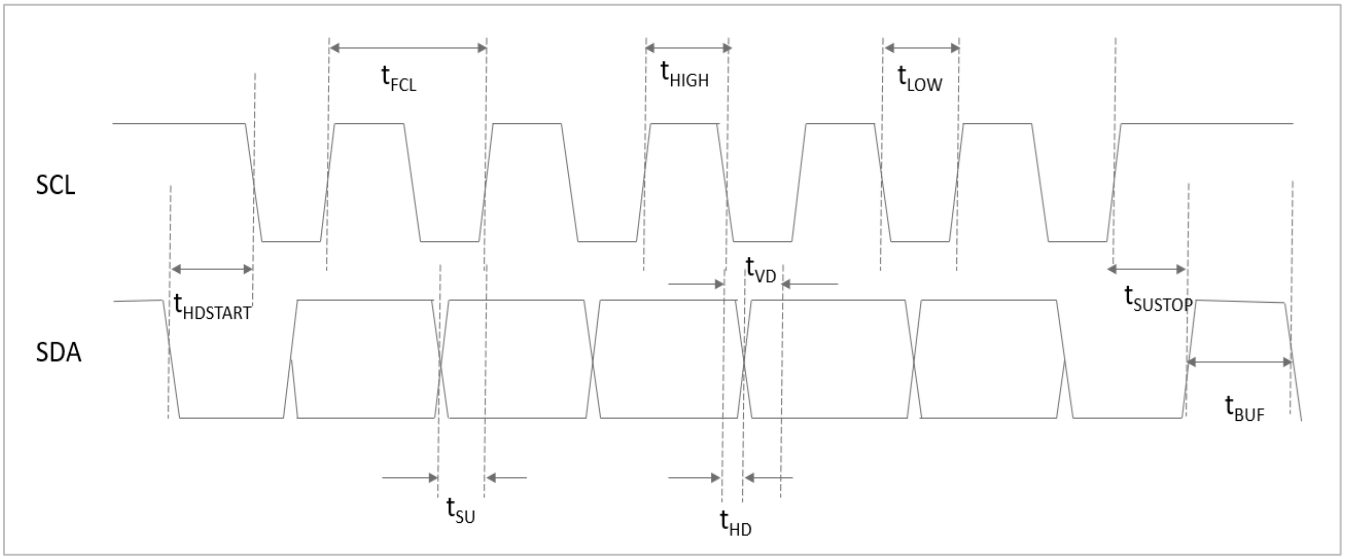


Figure 4. I²C Timing Diagram

Table 6. Environmental Compliance

Parameter	Test Condition	Value	Unit
Moisture Sensitivity Level (MSL)	MSL3 @260°C		
Soldering Temperature	MIL-STD-883, Method 2003	260	°C
Electrostatic Discharge (HBM)	JEDEC JS-001	2000	V
Charge-Device Model (CDM)	JEDEC JESD22-C101	500	V
Latch-up Compliance	JESD78 Compliant		

Table 7. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
5mm x 5mm 40 pin LGA	Maximum Board Temperature	T_B	125	°C
	Thermal Resistance, Junction to Ambient	$ø_{JA}$	36	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	14	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C

Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.

Table 8. Typical Output Phase Noise Characteristics
VDD= 1.8V, T_A = 25°C, Output Type = LVDS-EXT

Offset frequency	312.5 MHz	491.52 MHz	625 MHz	1250 MHz	Unit
1 KHz	-103	-98	-99	-93	dBc/Hz
10 KHz	-132	-130	-127	-122	dBc/Hz
100 KHz	-154	-152	-149	-143	dBc/Hz
1 MHz	-164	-160	-159	-152	dBc/Hz
10 MHz	-165	-161	-160	-151	dBc/Hz
20 MHz	-166	-161	-160	-153	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	22	22	20	22	fs

Typical Output Measured Phase Noise Plots

This section shows MS2508 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent E5052B Signal Source Analyzer.

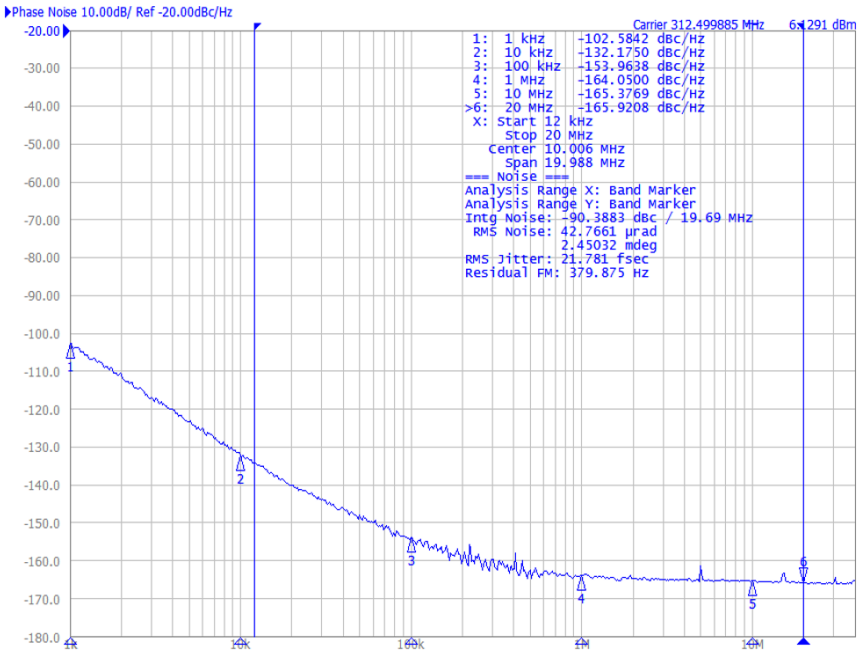


Figure 5. Center Frequency: 312.5 MHz

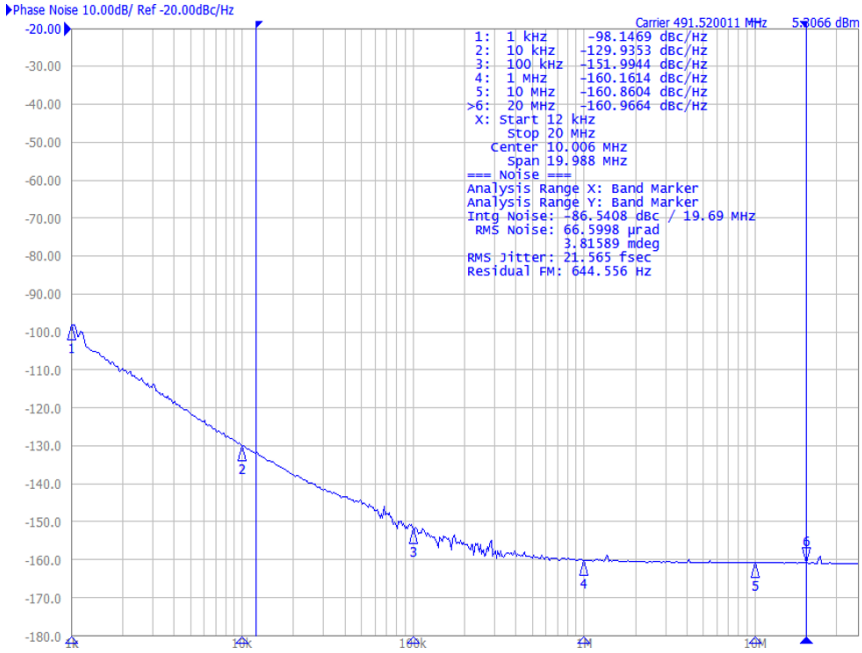


Figure 6. Center Frequency: 491.52 MHz

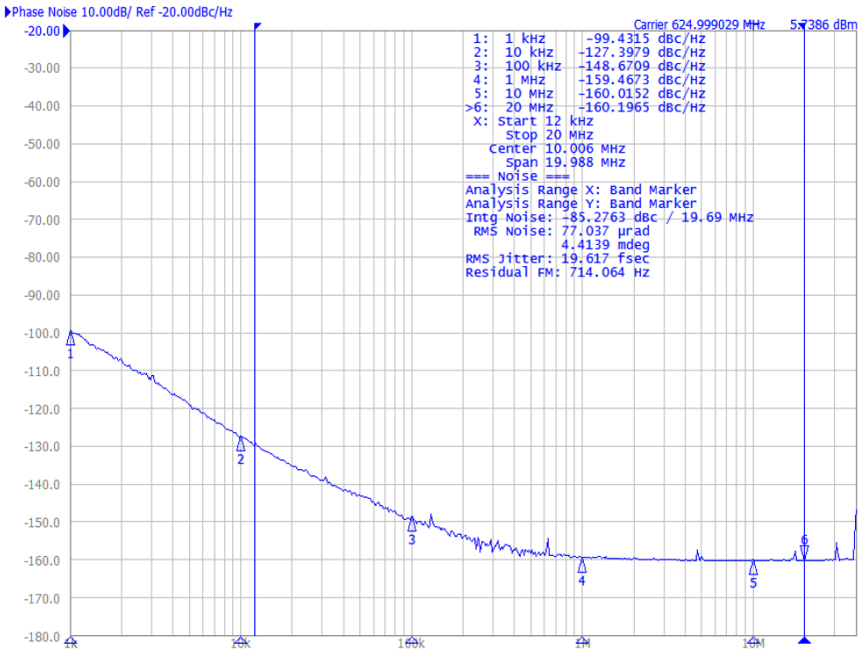


Figure 7. Center Frequency: 625 MHz

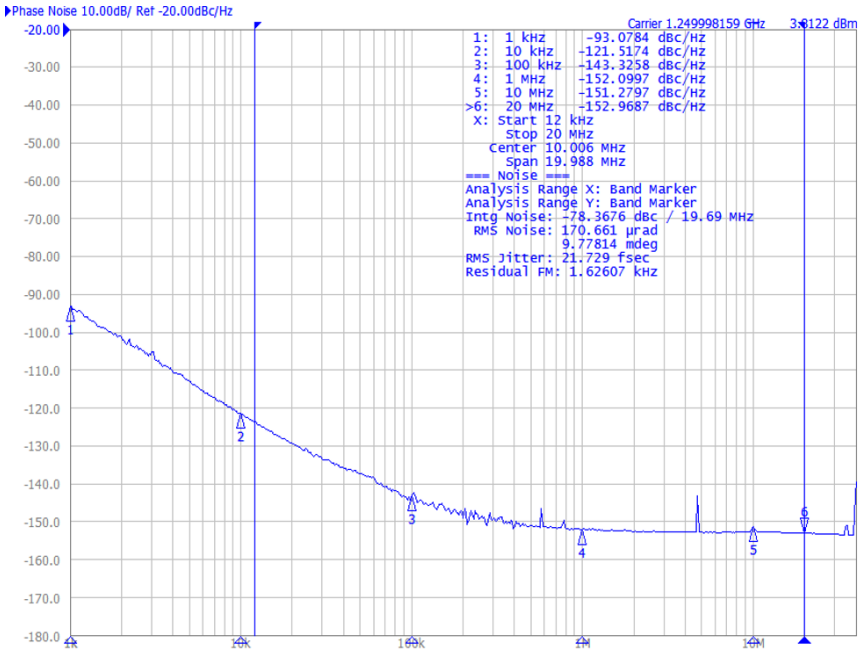


Figure 8. Center Frequency: 1250 MHz

Overview

The MS2508 is an eight-channel high-performance Jitter Attenuator that offers exceptional capabilities in the generation of an ultra-low phase noise clock, making it an ideal solution for next-generation communication systems and base stations. This device can produce eight differential output clocks synchronized to the reference clock input with input frequency ranging from 1MHz to 750MHz single-ended, and gapped clock support. The MS2508 boasts an output frequency range of 20MHz to 2.2GHz and a remarkably low RMS jitter of 25fs (12KHz to 20MHz), making it one of the most reliable and precise devices available.

The device's programmability is configured by on-chip non-volatile memory (NVM). This attribute permits the MS2508 to provide great flexibility and ease of use in a broad range of applications, including telecommunications, networking, and test and measurement equipment.

Functional Description

MS2508 is an all-digital clock generation device that incorporates a range of features to enable jitter attenuation and programmable multiplication of input frequency. It receives one reference clock input and generates any multiplication of the input clock using fractional multipliers and high-speed output dividers. The device can output various formats, such as LVDS, LVDS-EXT, CML, LVPECL, and HCSL.

1. Frequency Configuration
   The frequency configuration is defined through non-volatile memory (NVM). Device settings are programmed during manufacturing and are automatically loaded at power-up. A combination of fractional frequency synthesis (M/N) and integer output division (Rn) allows generation of a wide range of output frequencies across all outputs. Frequency planning parameters are calculated using the EZ-Cleaner™ GUI utility, which generates the required configuration values for NVM programming. Contact Mixed-Signal for the EZ-Cleaner™ GUI utility.

2. Jitter Attenuation Bandwidth Control
   The MS2508 provides digitally programmable jitter attenuation bandwidth control, which defines the degree of input reference jitter filtering. Bandwidth options from 0.01 Hz to 4 kHz are selectable during configuration and stored in NVM.
   Because jitter filtering and frequency synthesis are implemented entirely in the digital domain, the device maintains inherent stability across all supported bandwidth settings, with less than 0.1 dB of peaking, independent of the selected bandwidth.

Operation Modes

Free Running Mode (Default Mode)

After initialization, MS2508 will enter free running mode. In this mode, the device generates an output clock using multiplication factor stored in the on-chip NVM. The frequency accuracy of the generated output clock tracks the frequency accuracy of the input reference. For example, if the input frequency is 156.25 MHz (+/- 10ppm) and the stored multiplication factor is 33/32, the output frequency would be 161.1328125 MHz (+/- 10ppm).

Frequency Translation Example
For example, if the input frequency is 15.625 MHz (±10ppm) and the stored multiplication factor is 33/32, the resulting output frequency is:

$$F_{OUT} = F_{IN} \times (M/N)$$
$$Fout = 156.25\ MHz \times (33/32) = 161.1328125\ MHz$$

The output frequency tolerance directly tracks the input reference tolerance:

$$\Delta F_{OUT} = \Delta F_{IN}$$

Lock Acquisition Mode.

Upon completion of the configuration process, the MS2508 will transition into the lock acquisition mode. This mode comprises two stages: fast acquisition and narrow acquisition. In the first stage, the loop bandwidth is widened to facilitate a speedy initial acquisition process. Following this, the bandwidth is narrowed as the device completes the lock.

Output

MS2508 supports CML, LVDS, LVDS-EXT, LVPECL, and HCSL output formats. The output enable, OE, is active HI. When OE is LOW, MS2508 output will be High Z but the loop will stay locked.

Input Terminations (JA Mode)

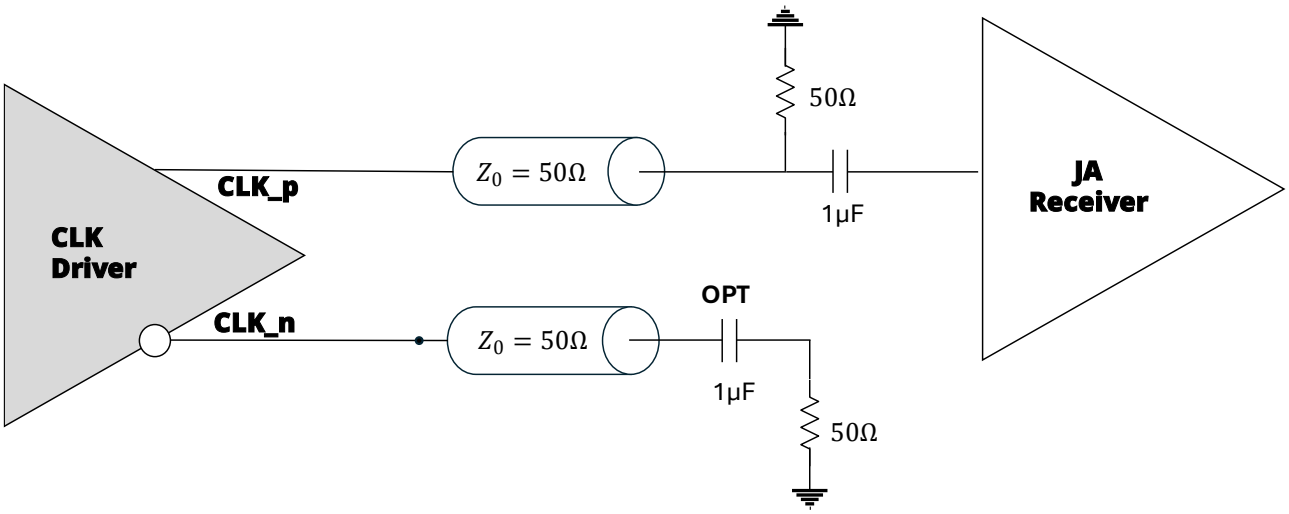


Figure 9. Differential Input Interface

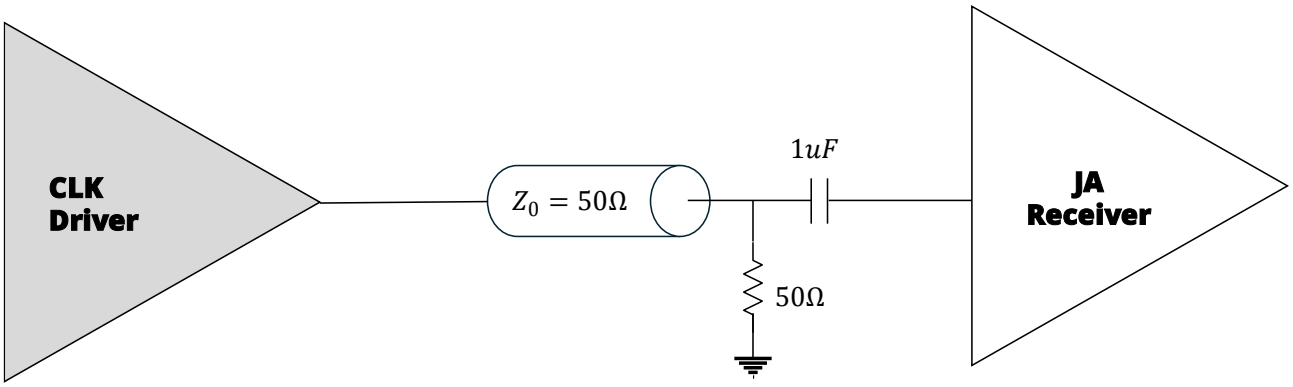


Figure 10. Single-Ended Input Interface

Output Terminations

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff
LVDS	0.7V	AC	100 Ω diff
LVDS-EXT	1.2V	AC	100 Ω diff
LVPECL	1.4V	AC	50 Ω to VT
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT
HCSL (Int Term)	1.35V	AC or DC	None
HCSL	1.35V	DC	50 Ω to GND

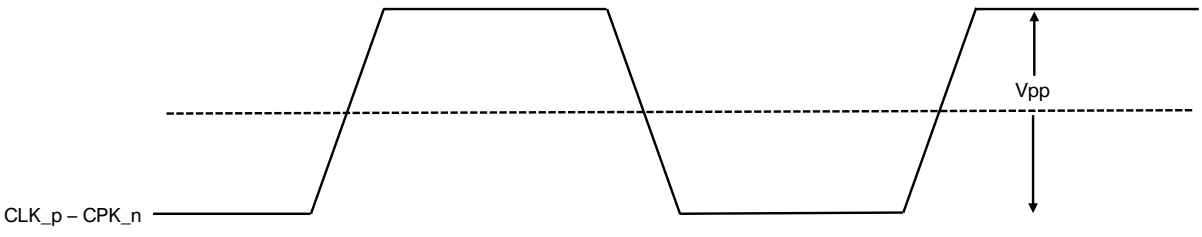


Figure 11. Differential Output Swing

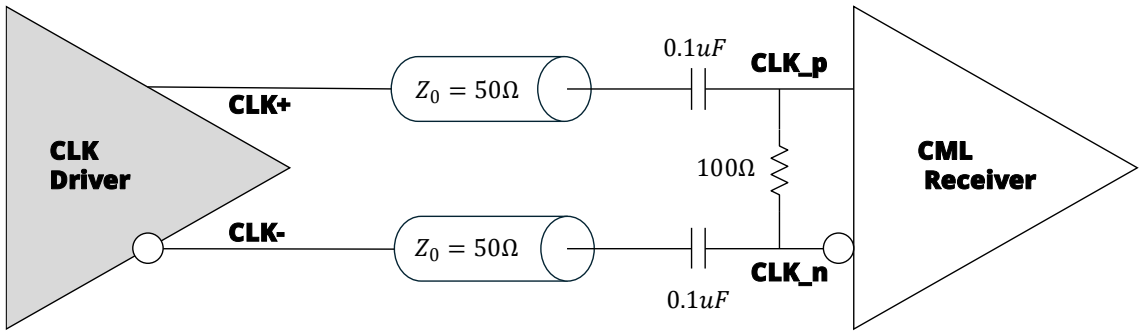


Figure 12. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

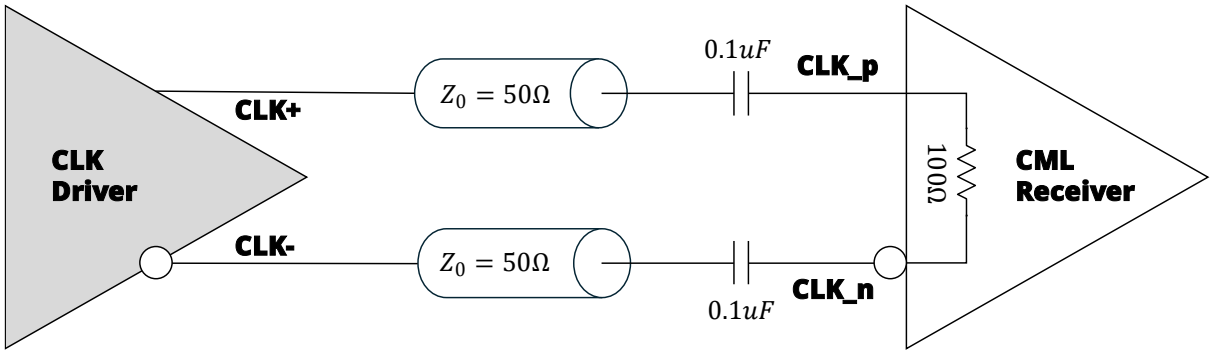


Figure 13. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

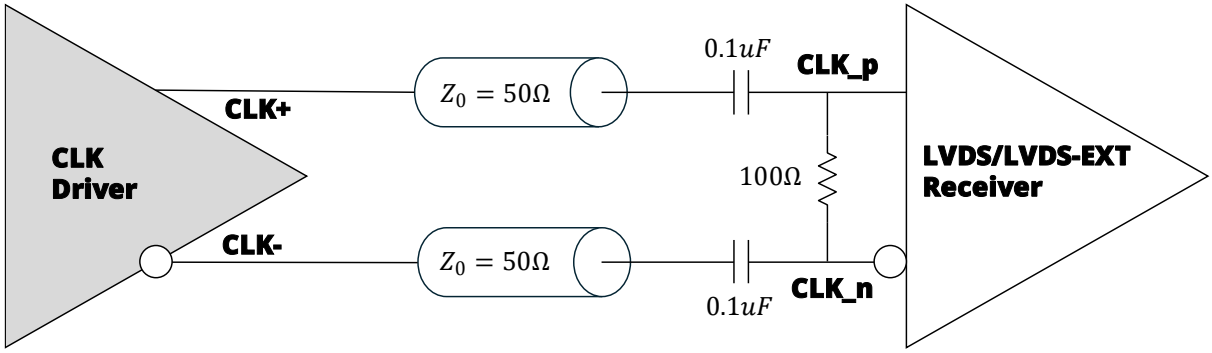


Figure 14. LVDS/LVDS-EXT Output Driver with 100 Ω Differential Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVDS/LVDS-EXT	0.7V/1.2V	AC	100 Ω diff

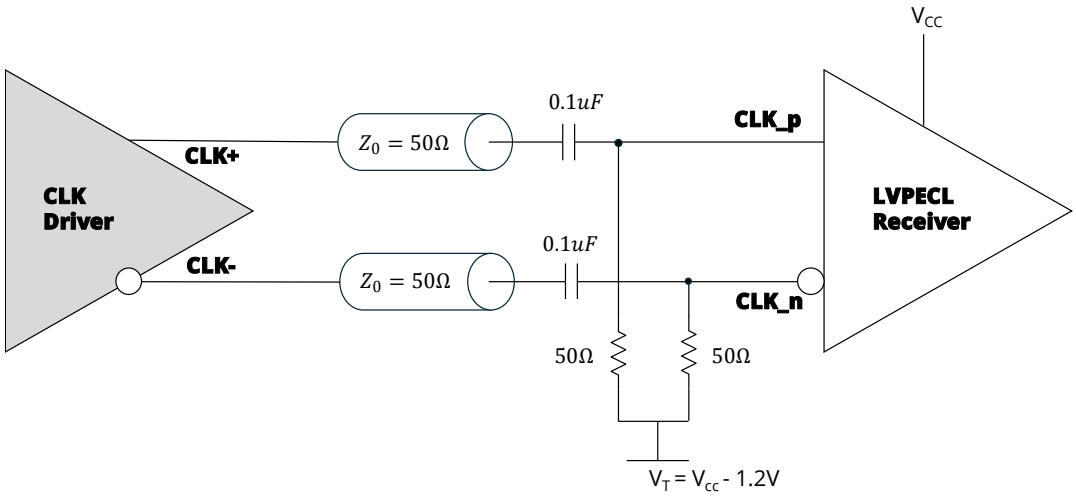


Figure 15. LVPECL Output Driver with External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL	1.4V	AC	50Ω to VT

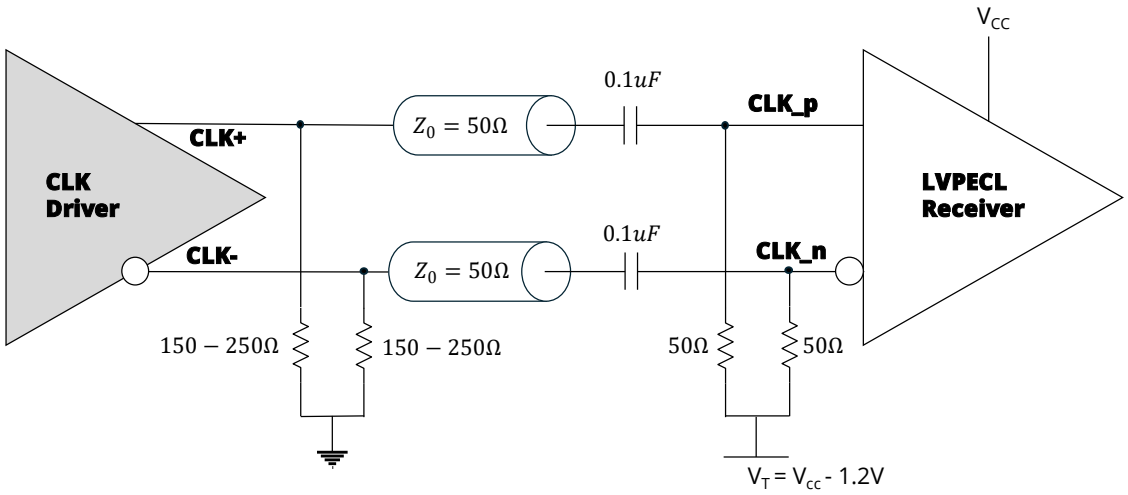


Figure 16. LVPECL Output Driver with Source Bias Resistors and External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT

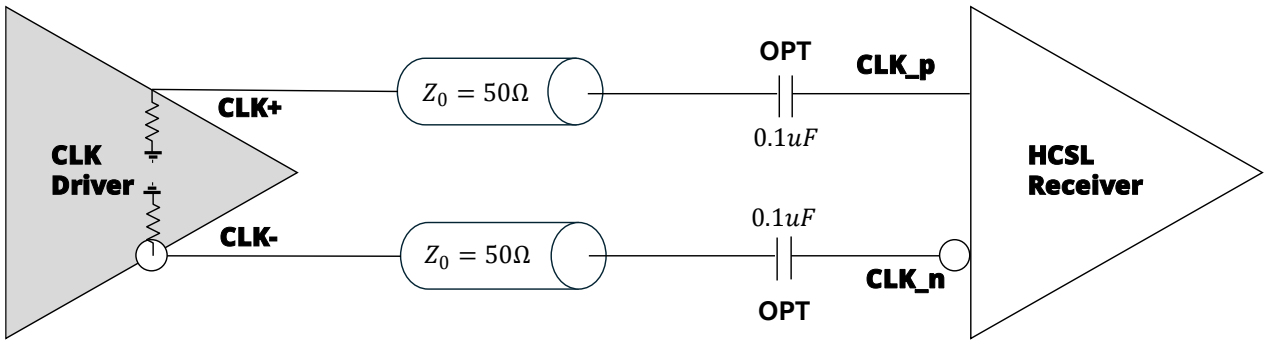


Figure 17. HCSL Output Driver with Integrated Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL (Int Term)	1.35V	AC/DC	None

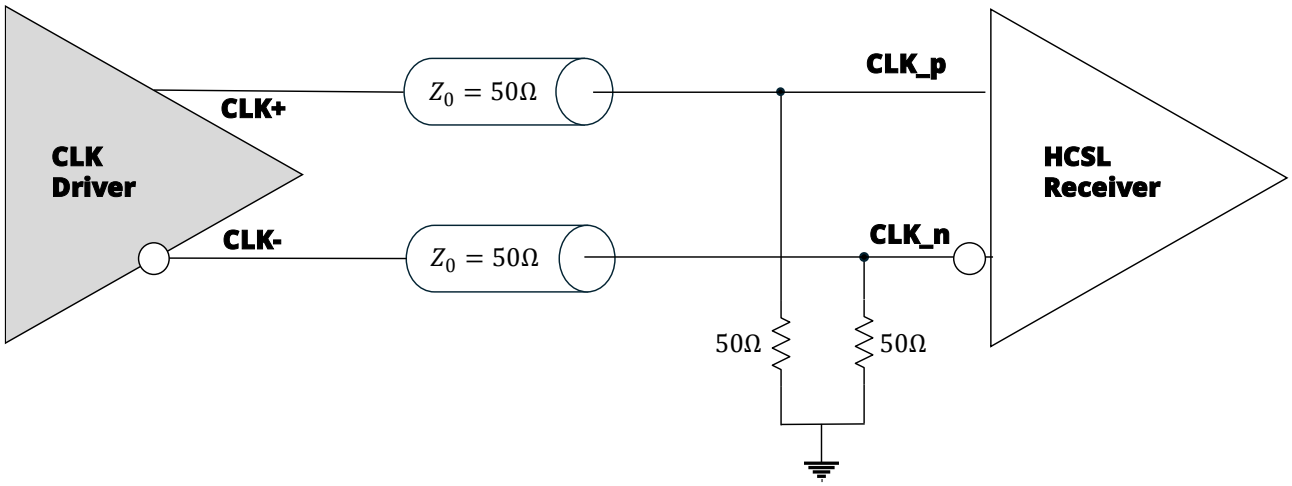


Figure 18. HCSL Output Driver with 50 Ω Receiver Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL	1.35V	DC	50 Ω to GND

Output Timing

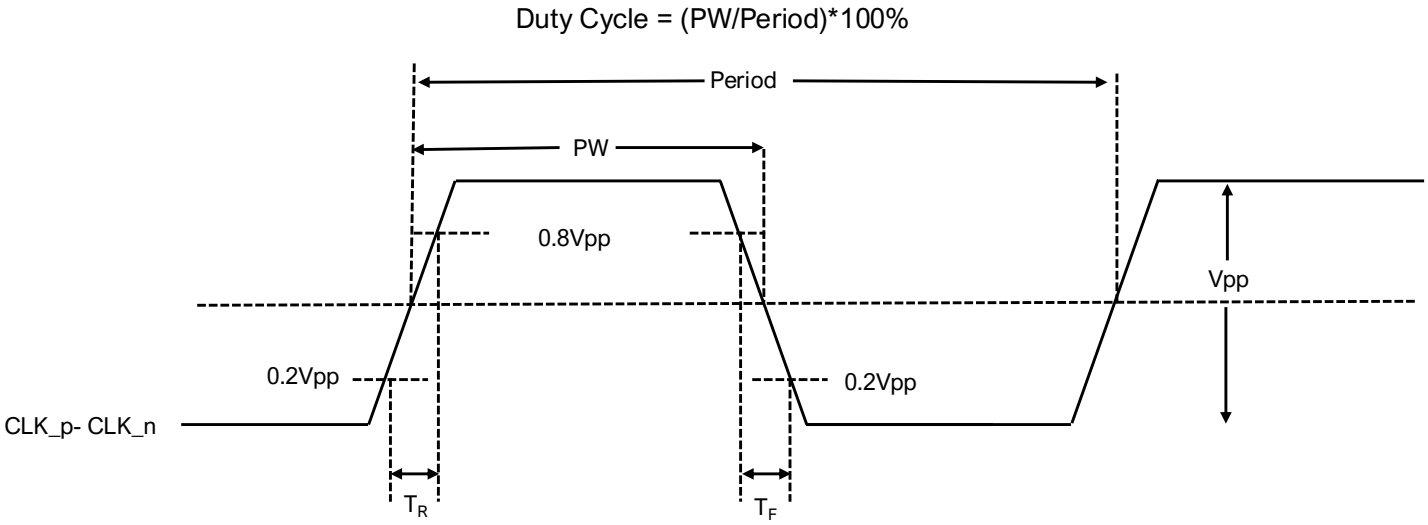


Figure 19. Output Timing across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps

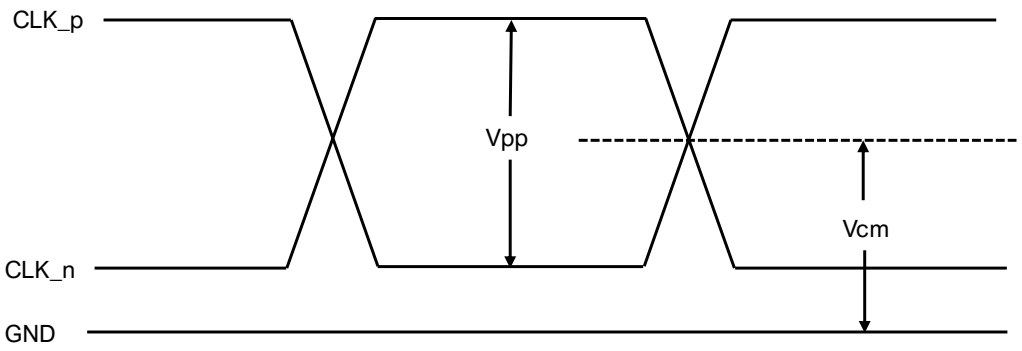


Figure 20. HCSL Output Level across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

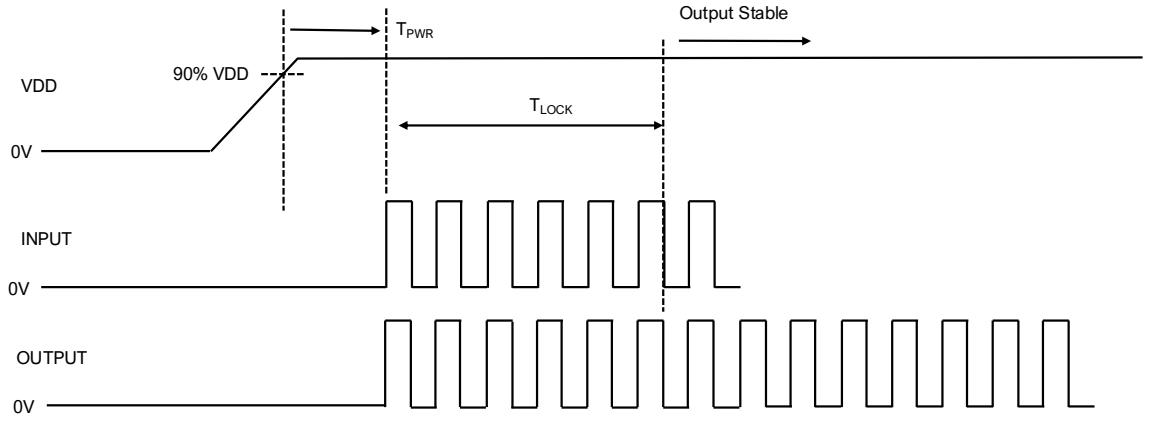


Figure 21. Powerup Timing Input/Output (JA Mode)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms
Output Lock Time	T_{LOCK}	Time from input signal to a stable output	10			ms

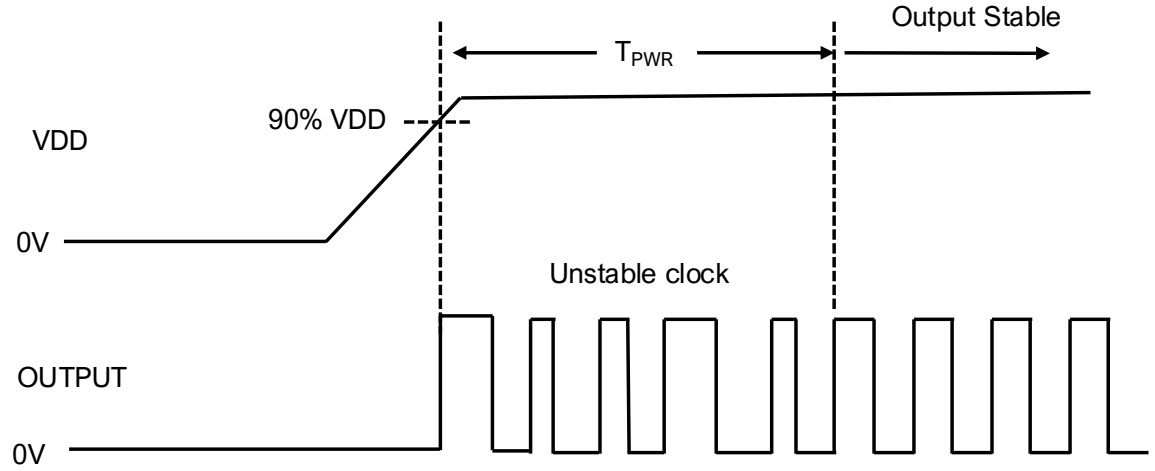


Figure 22. Powerup Timing (Clockgen Mode)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

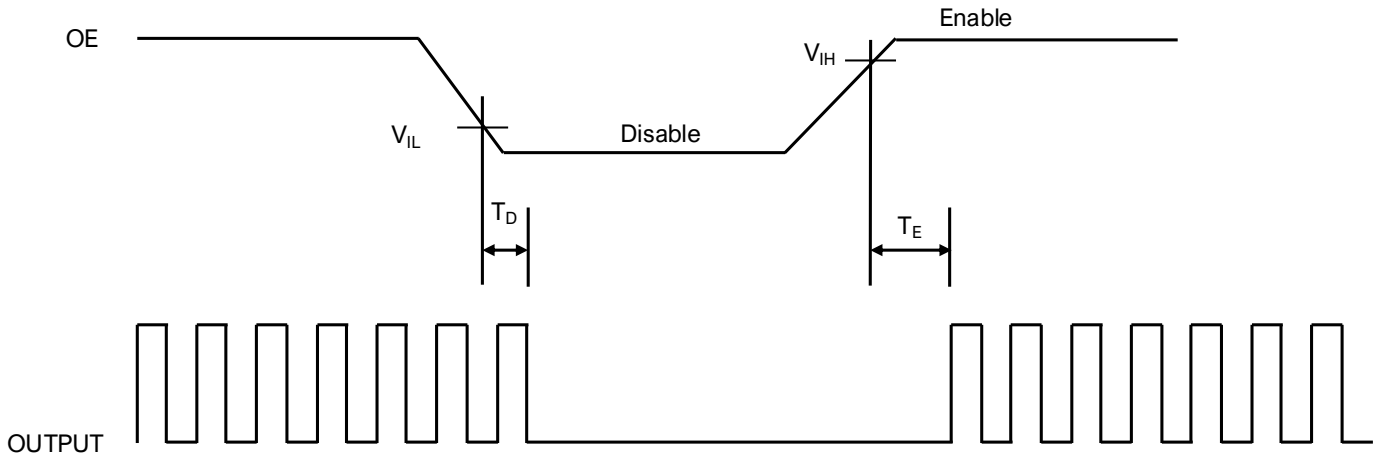


Figure 23. OE Enable/Disable Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs

Packaging Information

Figure 24 shows the MS2508 packaging drawing.

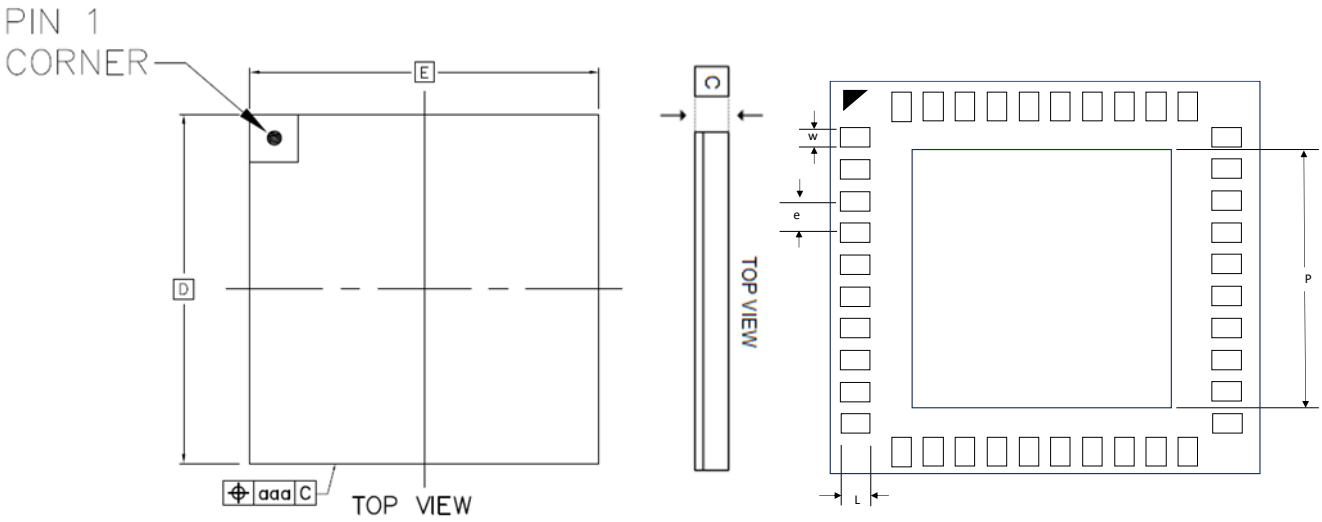


Figure 24. MS2508 Packaging Drawing (5X5, 40LGA)

Table 9. Package Dimensions

	SYMBOL	MIN	NOM	MAX
Total Thickness	C	0.896	0.946	0.996
Body Size	D		5 BSC	
	E		5 BSC	
Exposed Pad	P	3.5	3.6	3.7
Lead Pitch	e		0.4 BSC	
Lead Width	W	0.15	0.20	0.25
Lead Length	L	0.30	0.40	0.50
Package Edge Tolerance			0.1	
Mold Flatness			0.2	
Coplanarity			0.08	

Packaging Land Pattern

Figure 25 shows the MS2508 PCB land pattern.

Note: All dimensions are in millimeters

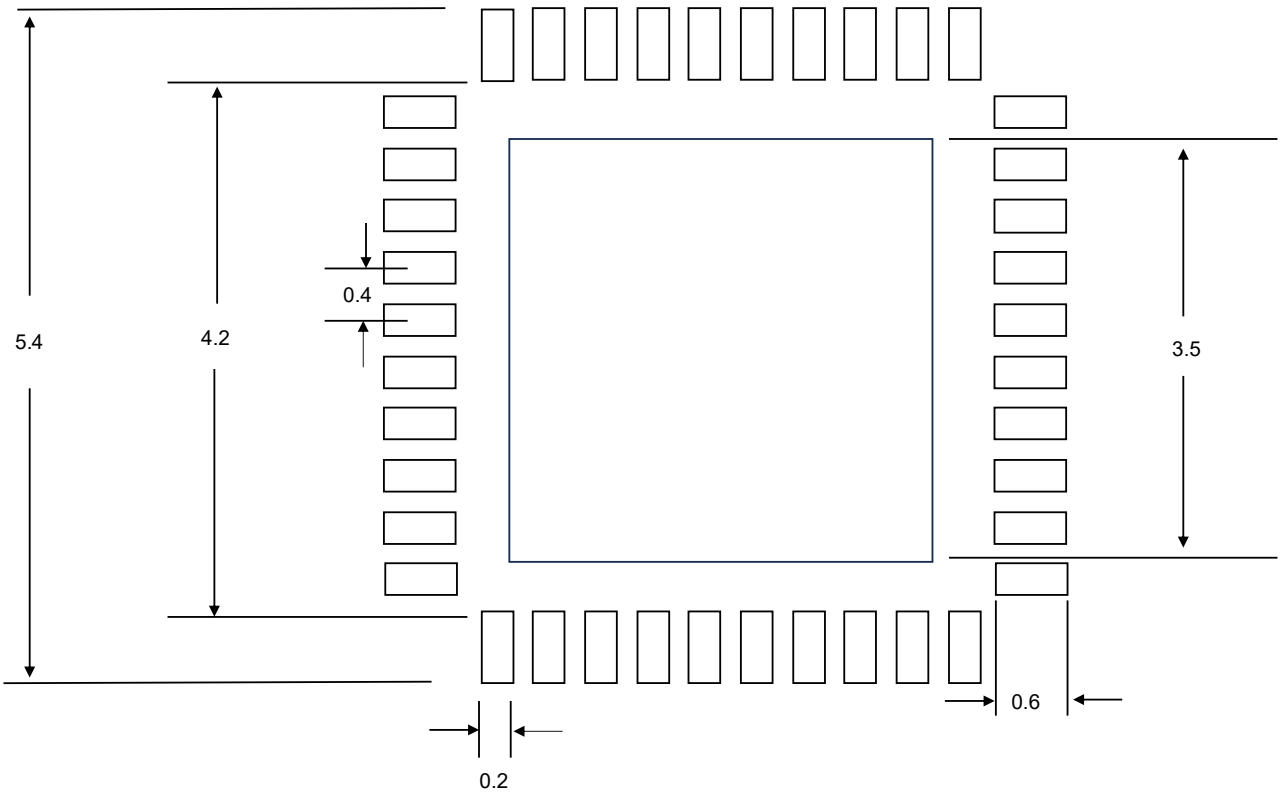


Figure 25. MS2508 Packaging Land Pattern Drawing (5X5, 40LGA)

Device Top Marking

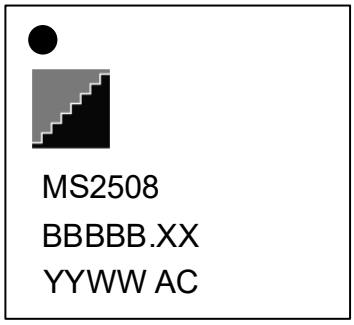


Figure 26. MS2508 Device Top Marking Showing Pin 1

Table 10. MS2508 Device Marking Legend

Line	Position	Description
1	1	Pin 1 Orientation Mark (Dot)
2	1	Mixed-Signal Logo
3	1-6	Product Marking
4	1-5	Wafer Lot Number
	6-7	Wafer #
5	Lot Trace Code	
	1-2	Year (last two digits of the year)
	3-4	Calendar Work Week Number (1-53)
	5-6	Assembly Code

Reflow Profile (IPC/JEDEC-STD-020)

Figure 27 shows the reflow profile for MS2508

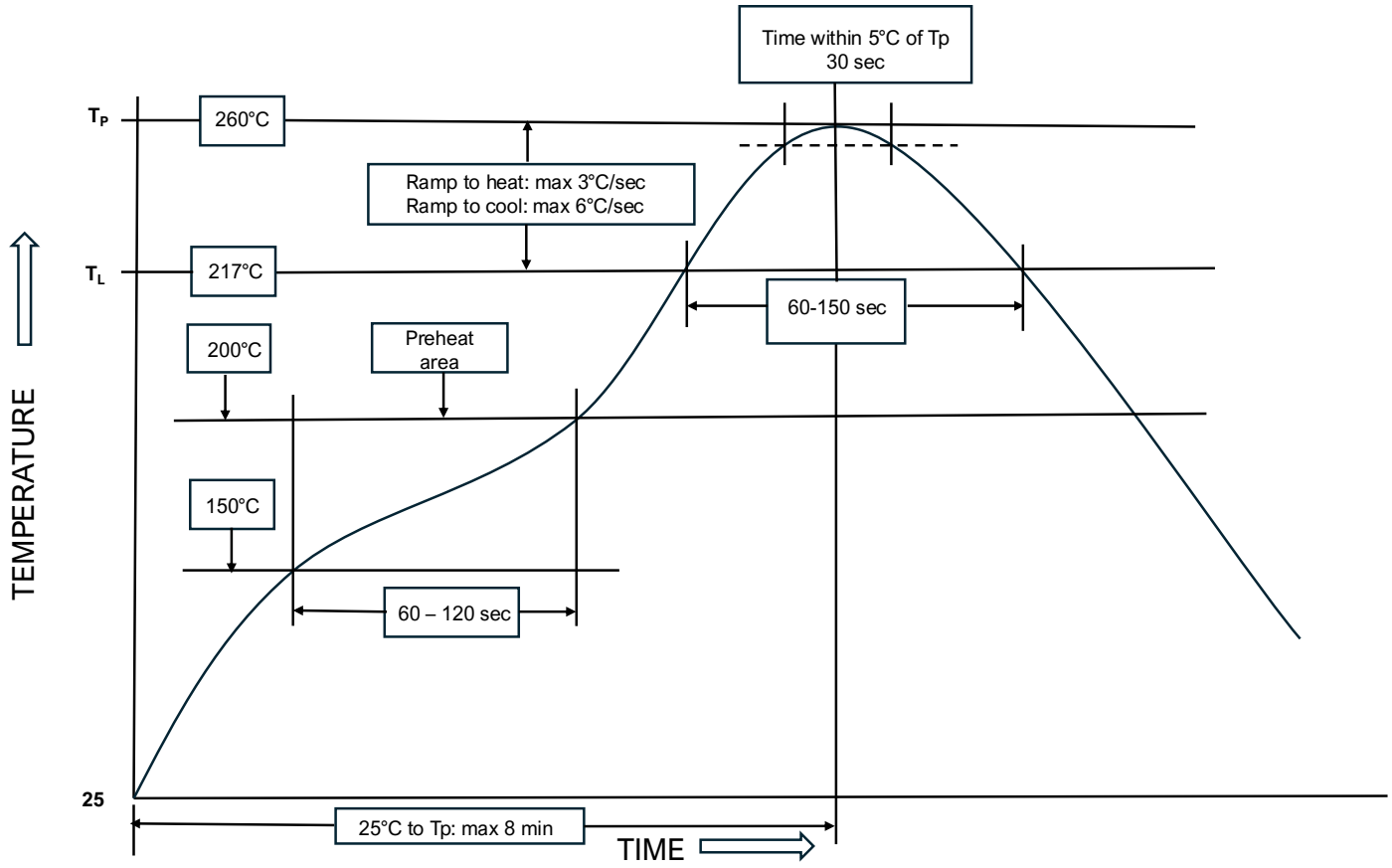


Figure 27. MS2508 Reflow Profile

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