MS2008

High-Performance Eight Outputs Programmable Clock Generator

Features

- Available at any frequency from 20 MHz to 2200 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 22 fs at 312.50 MHz
  - 22 fs at 491.52 MHz
  - 20 fs at 625 MHz
  - 22 fs at 1250 MHz
- Total stability of ±20 ppm
- Output Formats: LVDS/CML/LVPECL/HCSL/LVDS-EXT
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Industry standard 5X5 mm 40-pin LGA package
- Spread Spectrum for EMI attenuation
- 100Ω output impedance
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- I^2C Interface
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- Datacenter, Switches, Routers, NIC
- High-Speed Networking, 200G-1.6T
- Acceleration / AI, and Compute Nodes
- PCIe Gen.6, nVLink, Ethernet, Optical

General Description

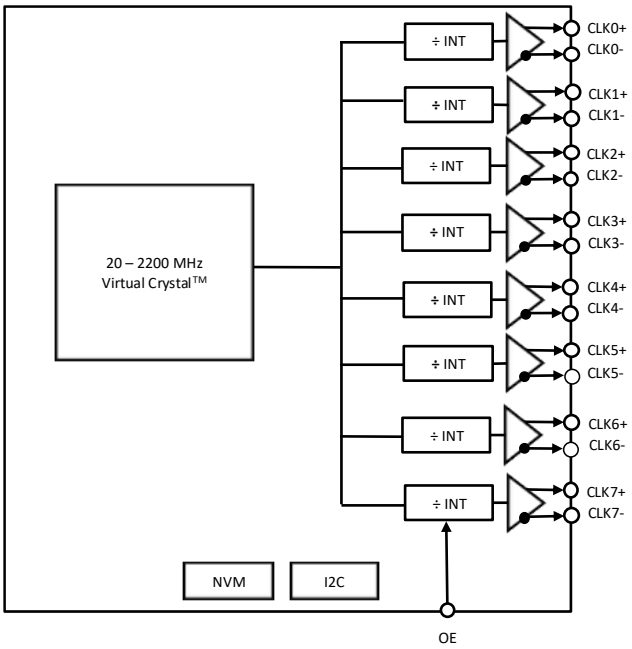
The MS2008 is a low-power, high-performance programmable clock generator. It provides eight differential outputs from a single clock domain. MS2008 can provide any frequency from 20 MHz to 2.2 GHz.

The product can be factory programmed using non-volatile memory (NVM), which becomes the default frequencies at power up. It can also be configured using I^2C interface.

Device Information

Part Number	Package	Description
MS2008	5X5 mm 40-pin LGA	Clock Generator

Figure 1. Functional Block Diagram



Pin Assignment and Pin Descriptions

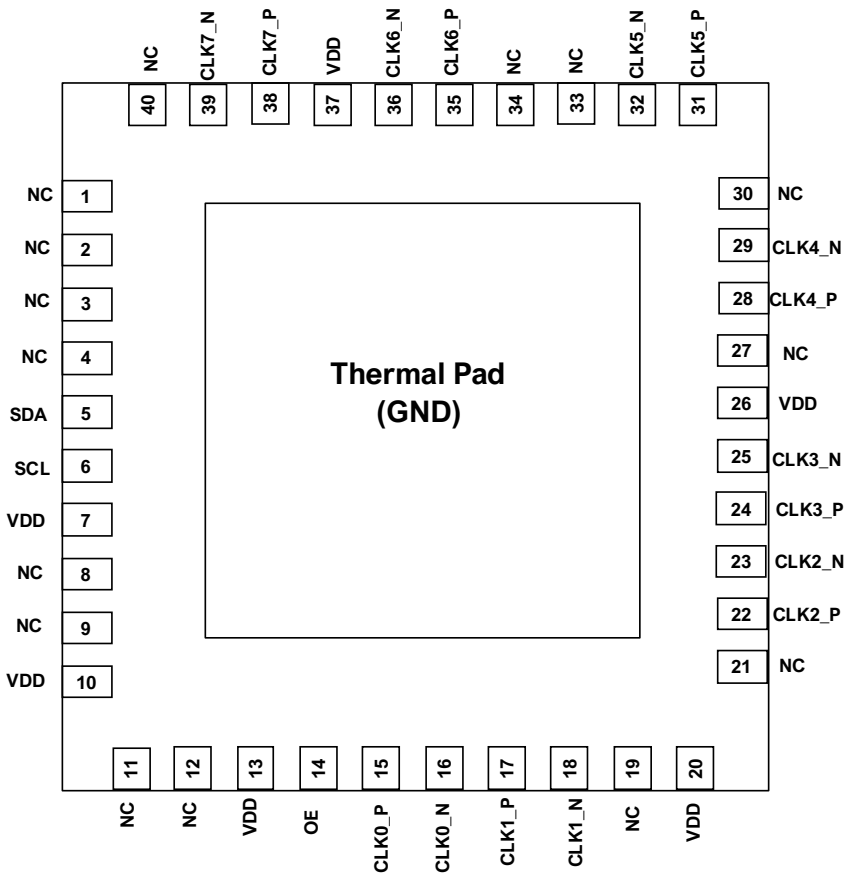


Figure 2. MS2008 Pin Assignments

Table 1. MS2008 Pin Descriptions

Pin No.	Name	I/O	Description
14	OE	I	Output Enable (All outputs)
5	SDA	I/O	I2C Serial Data
6	SCL	I	I2C Serial Clock
15	CLK0_P	O	Differential Clock Output
16	CLK0_N		
17	CLK1_P	O	Differential Clock Output
18	CLK1_N		
22	CLK2_P	O	Differential Clock Output
23	CLK2_N		
24	CLK3_P	O	Differential Clock Output
25	CLK3_N		
28	CLK4_P	O	Differential Clock Output
29	CLK4_N		
31	CLK5_P	O	Differential Clock Output
32	CLK5_N		
35	CLK6_P	O	Differential Clock Output
36	CLK6_N		
38	CLK7_P	O	Differential Clock Output
39	CLK7_N		
7,10,13,20,26,37	VDD	POWER	1.8V Power Supply
1,2,3,4,8,9,11,12,19,21,27,30,33, 34 ,40	NC		No Connect
Thermal Pad (GND)	GND	POWER	Device GND, Thermal Pad

Part Ordering Information

Figure 3 shows a logic tree for ordering each of the available parts.

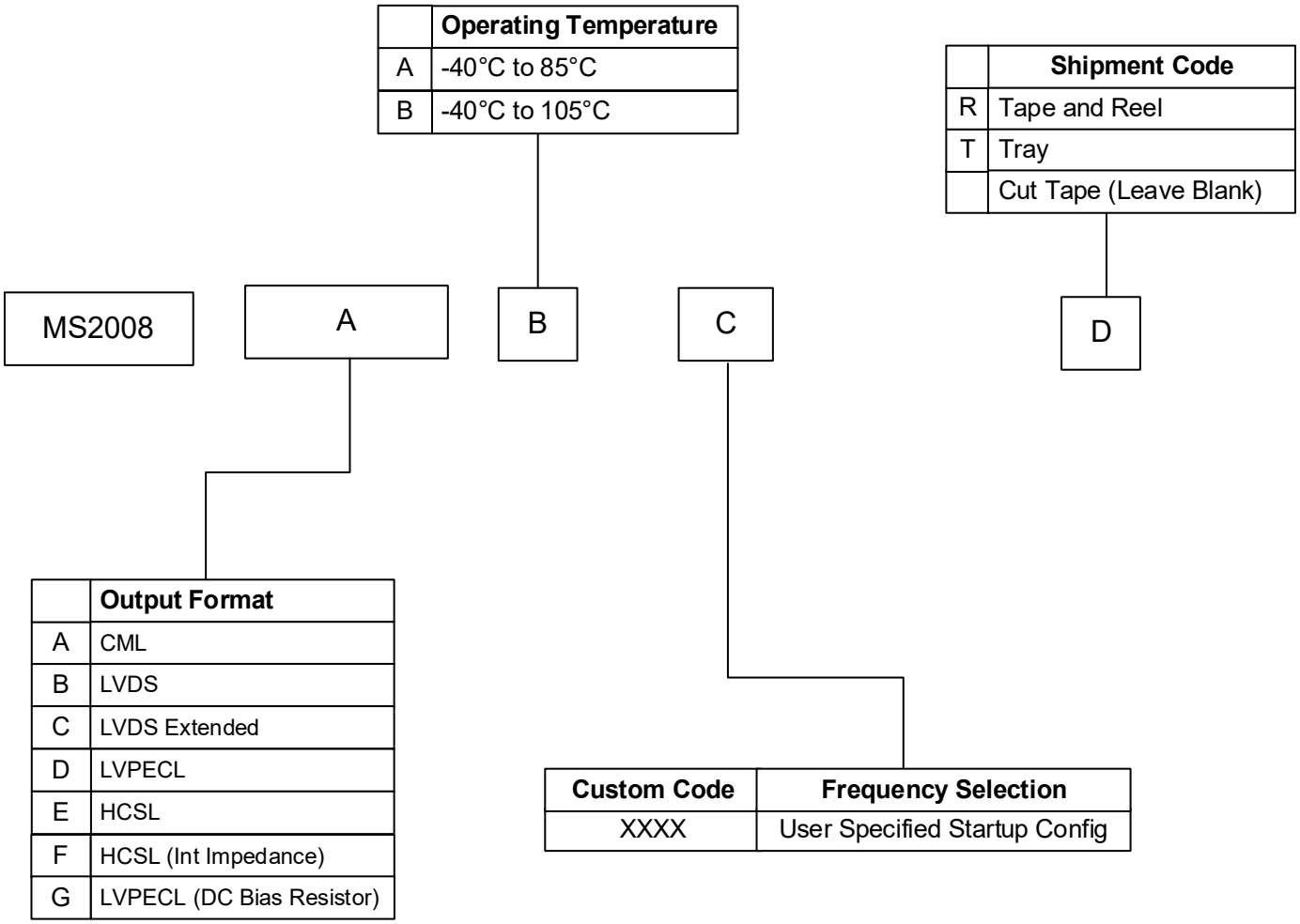


Figure 3. MS2008 Part Ordering Information

Table 2. Example of ordering part number

Base P/N	Output format	Operating Temperature	Frequency Code	Shipment Type	**Ordering part number**
MS2008	LVDS	-40°C to 85°C	0001*	Tape and Reel	**MS2008BA0001R**

* Frequency Code table will be provided by factory based on customer requirements.

Specifications

Table 3. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard output terminations (See Figure 9-15). A 0.1uF and 10uF bypass capacitors should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Frequency Range	F_{CLK}	All Output Formats	20		2200	MHz
Frequency Stability						
Frequency Stability*	F_{STB}		-20		20	PPM
*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year, +25°C). Aging is estimated from environmental reliability tests;						
Clock Output Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz integration band)	Φ_{JITTER}	Frequency=491.52 MHz		22	33	fs
		Frequency=625 MHz		20	30	fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		1.71 (-5%)	1.8	1.89 (+5%)	V
Temperature Range	T_A	Industrial Temperature	-40	25	85	°C
		Extended Industrial Temperature	-40	25	105	°C

Current Consumption

Supply Current Consumption	I_{DD}	LVDS Output (Output Enabled)		160	190	mA
		All Other Outputs (Output Enabled)		150	180	mA
		Tristate Hi-Z (Output Disabled. OE=0)		70	84	mA

Input Characteristics

Digital Input Levels(OE/SDA/SCL)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10 Char data	ms

PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (1) (Center Frequency is 312.5MHz)		-110		dBc
Power Supply-Jitter Sensitivity	PSJS			0.2		fs/mV

Note:

(1) Measured with 50 mVpp ripple from 500 KHz to 10 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps
CML Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 10, Figure 11	0.6	0.8	1	V
LVDS Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 12	0.5	0.7	0.9	V
LVDS-EXT Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 12	0.8	1.2	1.6	V
LVPECL Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 13, Figure 14	1.2	1.4	1.6	V
HCSL Output (AC or DC-Coupled)	Vpp	Differential Pk-Pk See Figure 15, Figure 16	1.1	1.35	1.6	V
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV
Output-Output Crosstalk	XTALK	Measure spur from adjacent output		-75		dBc

Unless otherwise specified, all differential output amplitudes are measured across a 100 Ω differential load or the termination network shown in the referenced output driver figures on the following pages

Table 4. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O (OE/SDA/SCL)	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Junction Temperature		150	°C
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

I2C Interface

Table 5. I²C Timing Specifications
VDD=1.8V +/-5%, Ta= Operating Temperature

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Units
SCL Clock Frequency	tFCL			100	400	KHz
Data Set-up Time	tSU		80			ns
Data Hold Time	tHD		0			ns
Data Valid Time, Data Acknowledge Time	tVD		0.85			us
Hold time for START Condition	tHDSTART		0.5			us
Set-up time for STOP Condition	tSUSTOP		0.5			us
Low Period of SCL Clock	tLOW		1.2			us
High Period of SCL Clock	tHIGH		0.5			us
Bus Turnaround Time Between STOP and START Condition	tBUF		2			us
Note: SDA/SCL pins requires 470Ω pull-up resistor						

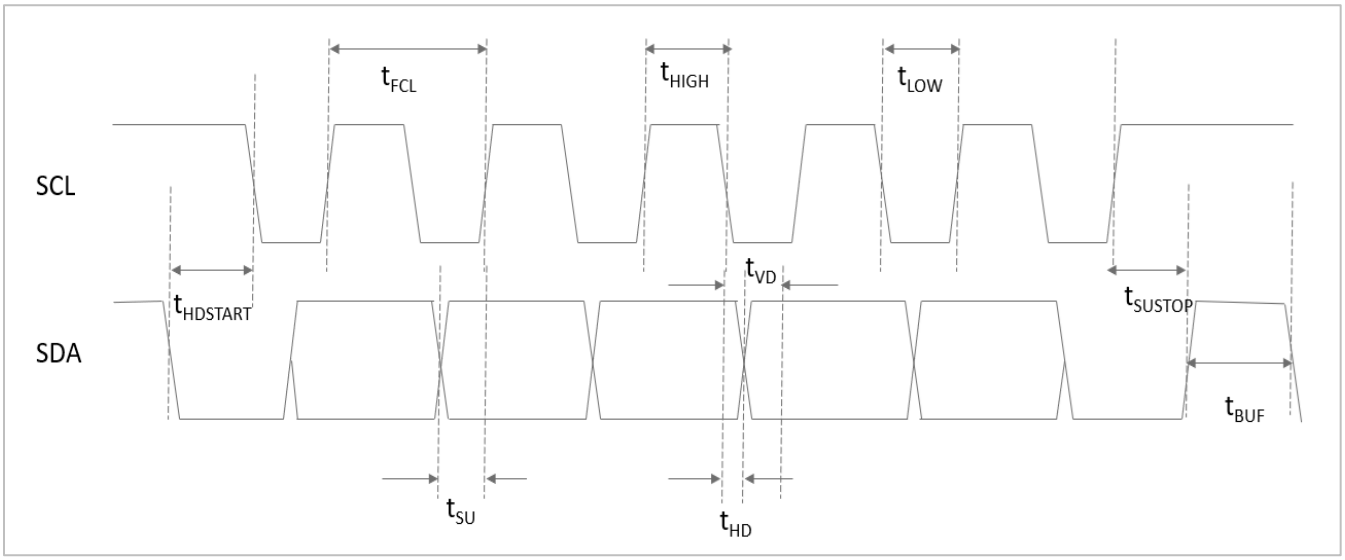


Figure 4. I²C Timing Diagram

Table 6. Environmental Compliance

Parameter	Test Condition	Value	Unit
Moisture Sensitivity Level (MSL)	MSL3 @260°C		
Soldering Temperature	MIL-STD-883, Method 2003	260	°C
Electrostatic Discharge (HBM)	JEDEC JS-001	2000	V
Charge-Device Model (CDM)	JEDEC JESD22-C101	500	V
Latch-up Compliance	JESD78 Compliant		

Table 7. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
5mm x 5mm 40 pin LGA	Maximum Board Temperature	T_B	125	°C
	Thermal Resistance, Junction to Ambient	$ø_{JA}$	36	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	14	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C
Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

Table 8. Typical Output Phase Noise Characteristics
VDD= 1.8V, T_A = 25°C, Output Type = LVDS-EXT

Offset frequency	312.5 MHz	491.52 MHz	625 MHz	1250 MHz	Unit
1 KHz	-103	-98	-99	-93	dBc/Hz
10 KHz	-132	-130	-127	-122	dBc/Hz
100 KHz	-154	-152	-149	-143	dBc/Hz
1 MHz	-164	-160	-159	-152	dBc/Hz
10 MHz	-165	-161	-160	-151	dBc/Hz
20 MHz	-166	-161	-160	-153	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	22	22	20	22	fs

Typical Output Measured Phase Noise Plots

This section shows MS2008 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent E5052B Signal Source Analyzer.

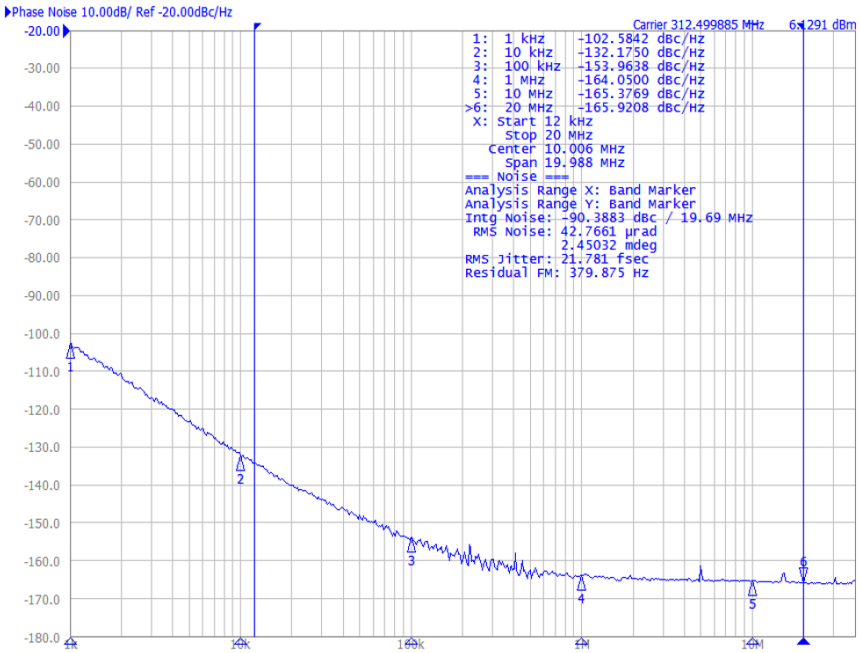


Figure 5. Center Frequency: 312.5 MHz

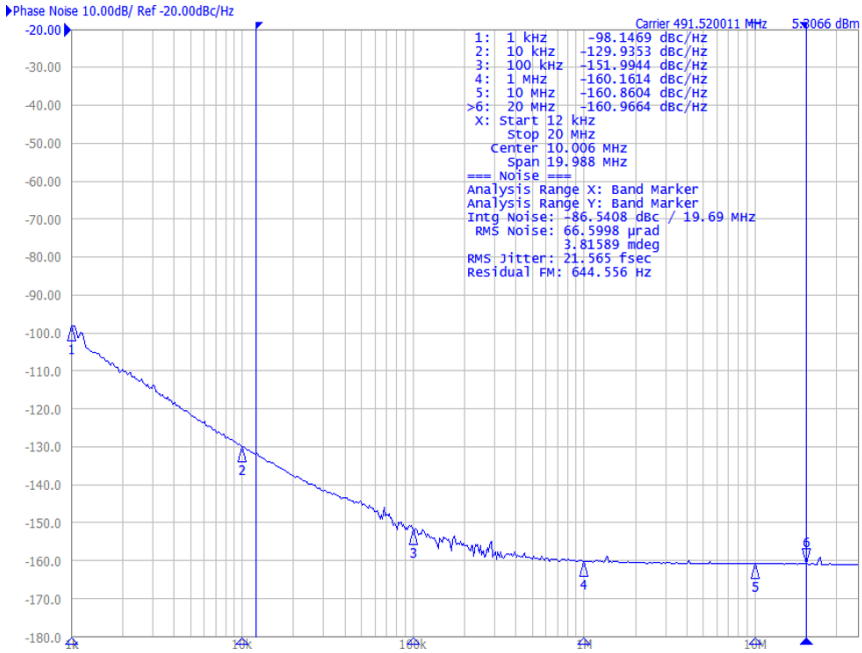


Figure 6. Center Frequency: 491.52 MHz

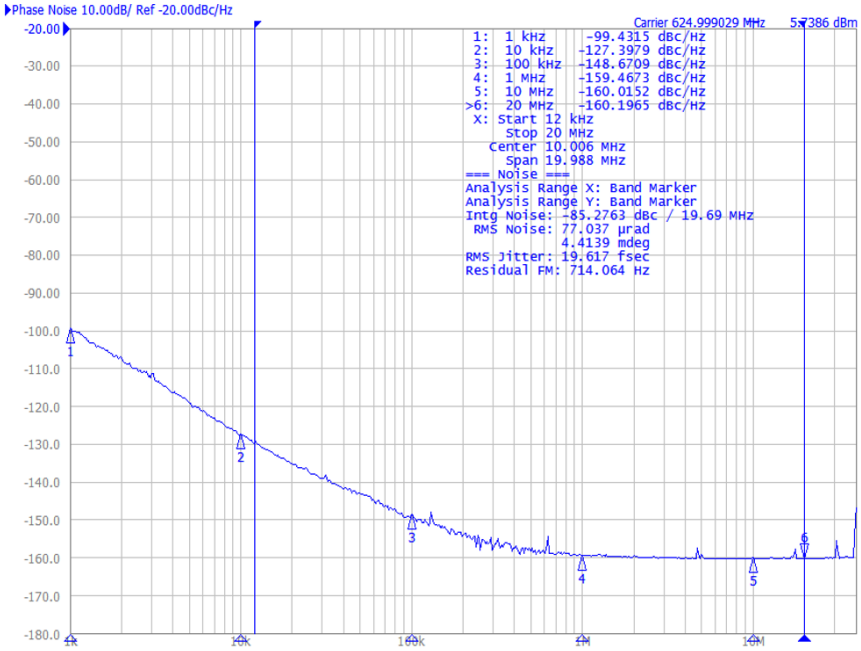


Figure 7. Center Frequency: 625 MHz

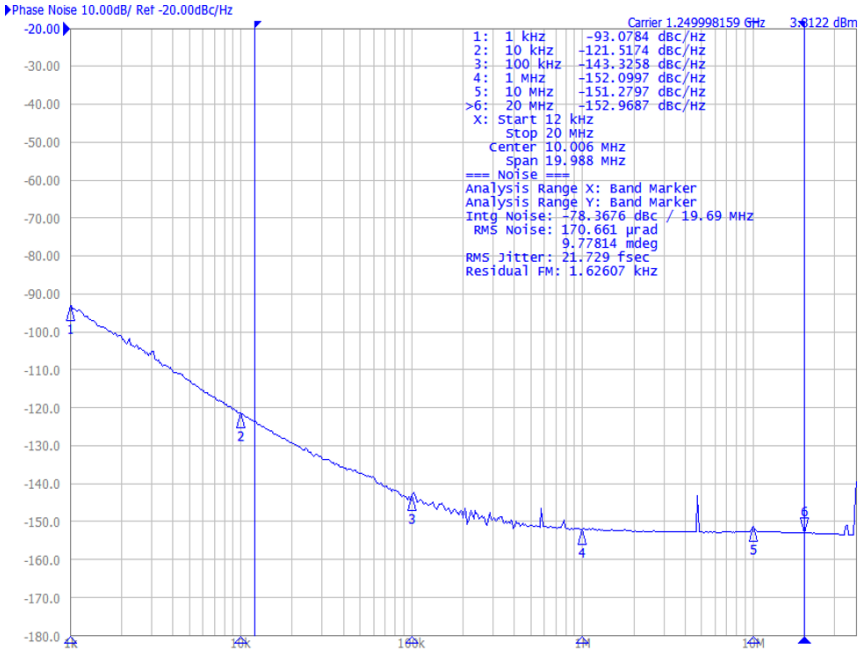


Figure 8. Center Frequency: 1250 MHz

Output Terminations

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff
LVDS	0.7V	AC	100 Ω diff
LVDS-EXT	1.2V	AC	100 Ω diff
LVPECL	1.4V	AC	50 Ω to VT
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT
HCSL (Int Term)	1.35V	AC or DC	None
HCSL	1.35V	DC	50 Ω to GND

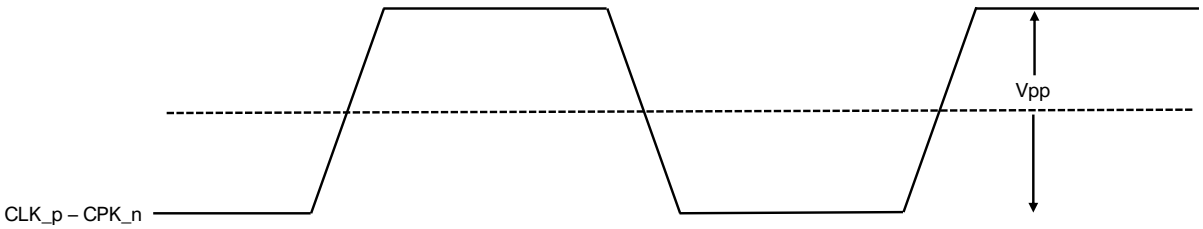


Figure 9. Differential Output Swing

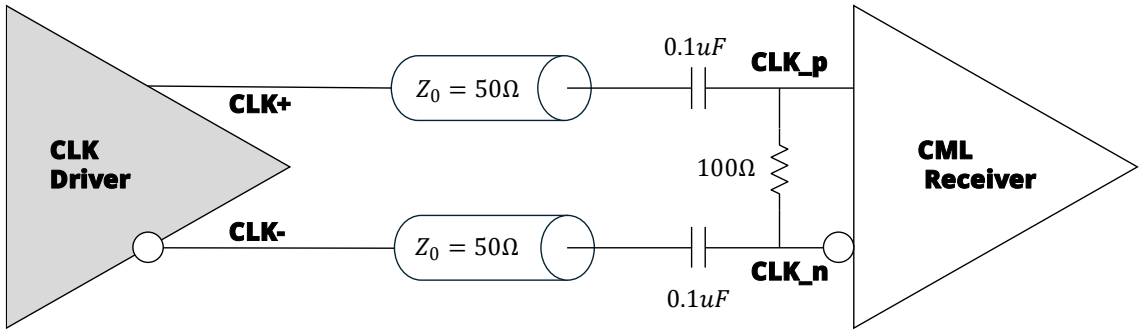


Figure 10. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

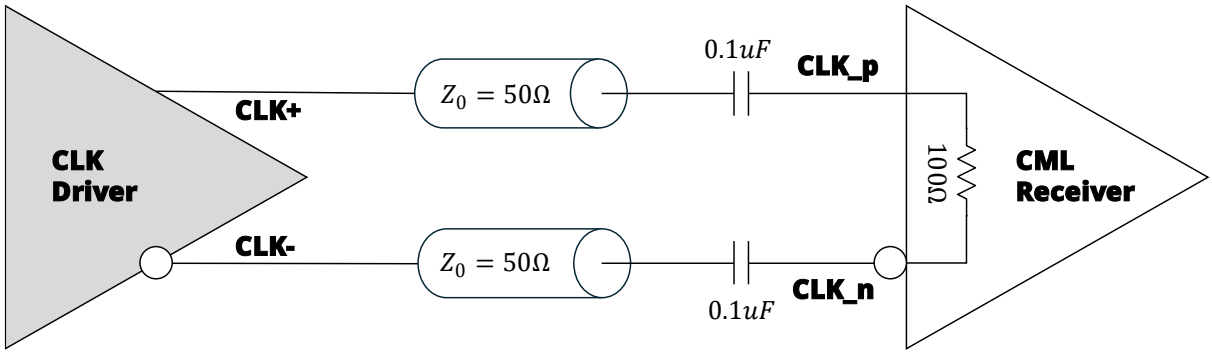


Figure 11. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

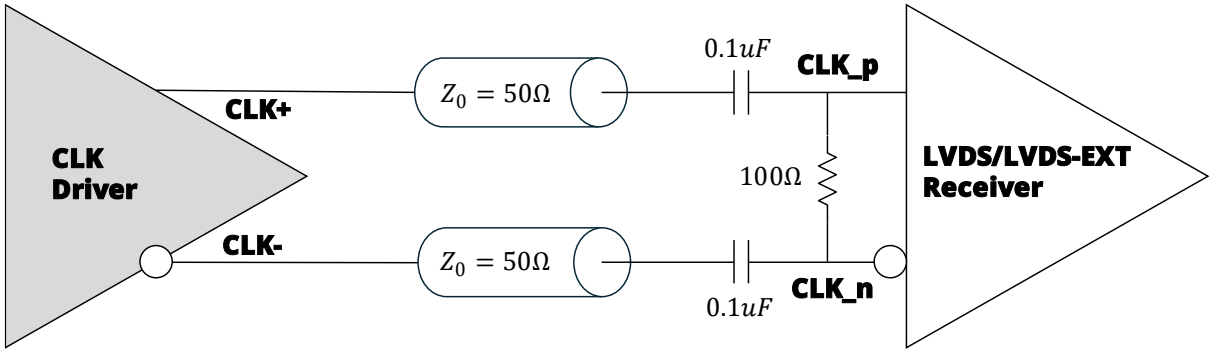


Figure 12. LVDS/LVDS-EXT Output Driver with 100 Ω Differential Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVDS/LVDS-EXT	0.7V/1.2V	AC	100 Ω diff

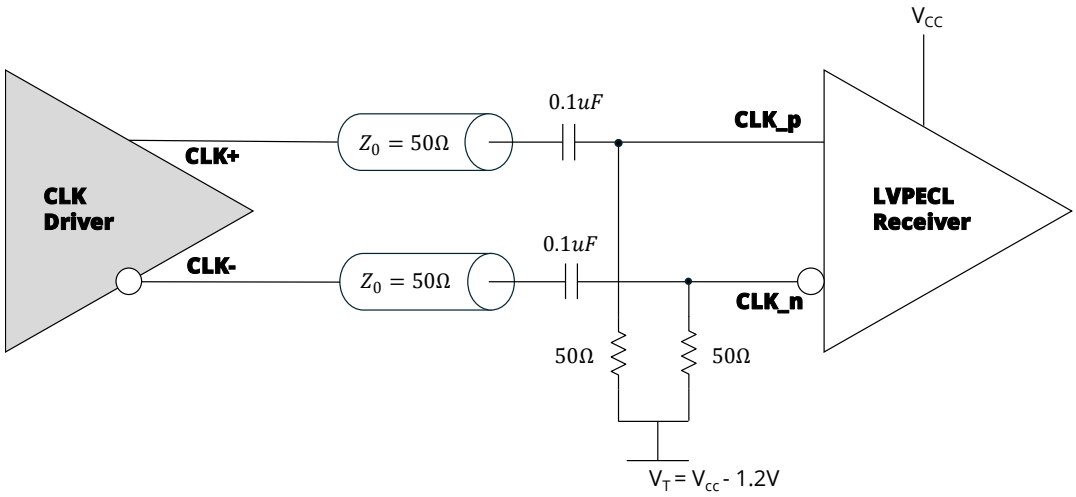


Figure 13. LVPECL Output Driver with External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL	1.4V	AC	50Ω to VT

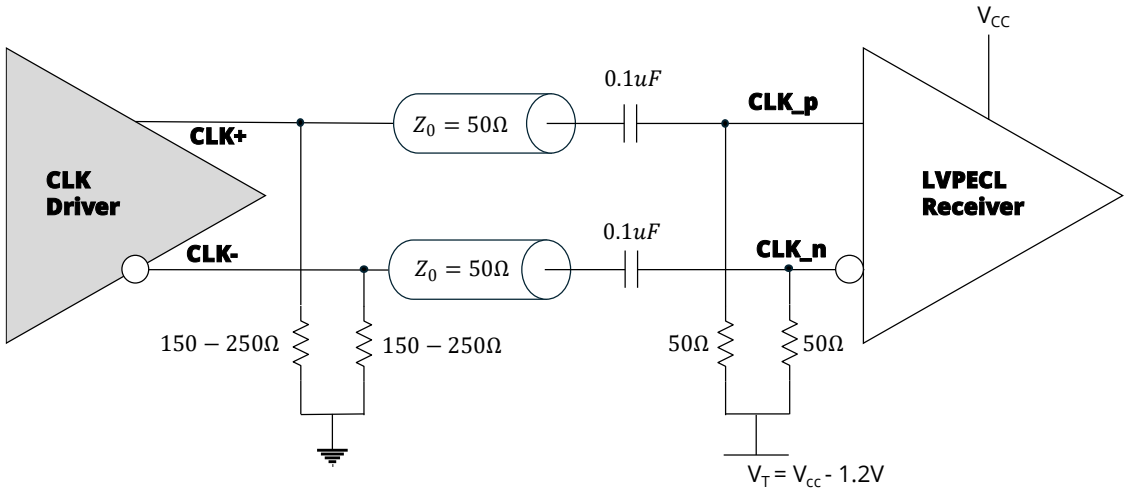


Figure 14. LVPECL Output Driver with Source Bias Resistors and External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT

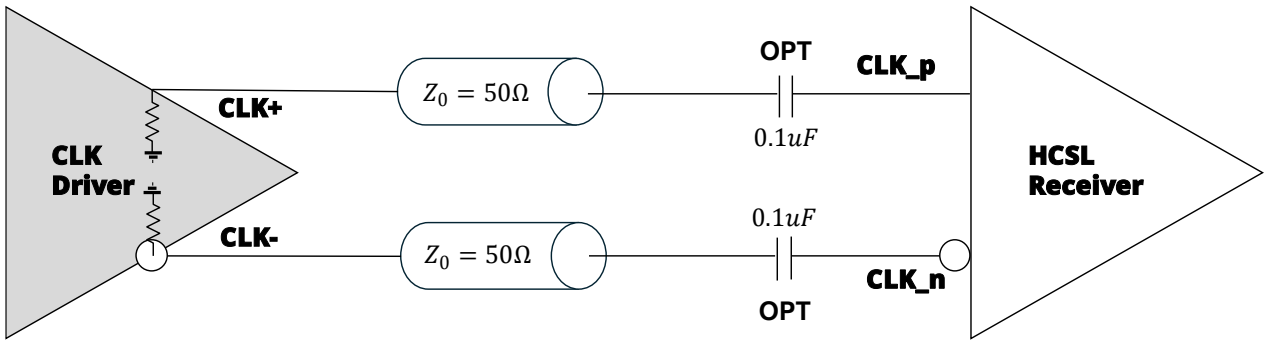


Figure 15. HCSL Output Driver with Integrated Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL (Int Term)	1.35V	AC/DC	None

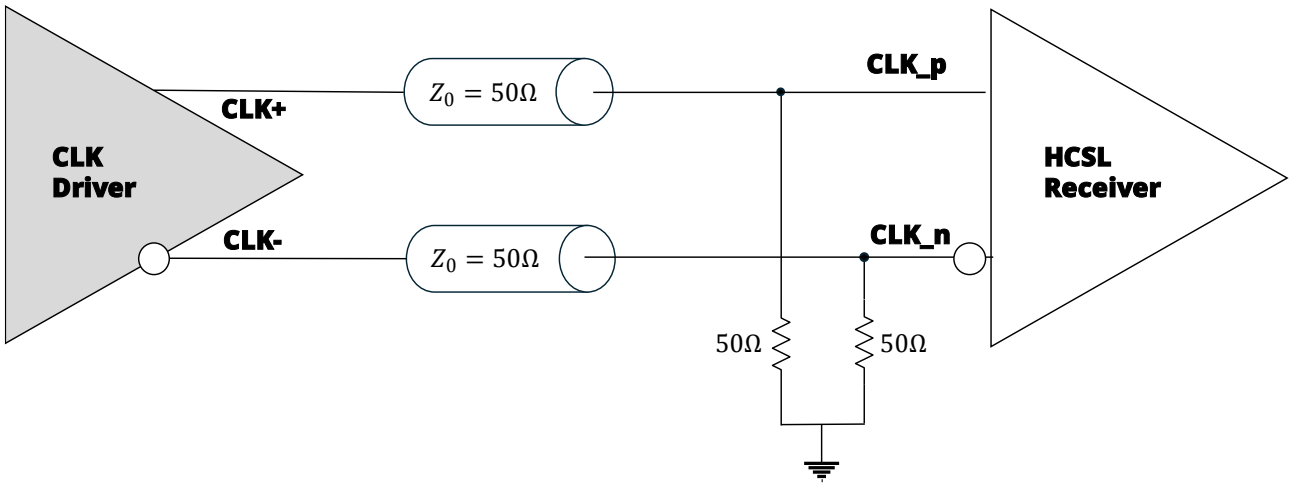


Figure 16. HCSL Output Driver with 50 Ω Receiver Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL	1.35V	DC	50 Ω to GND

Output Timing

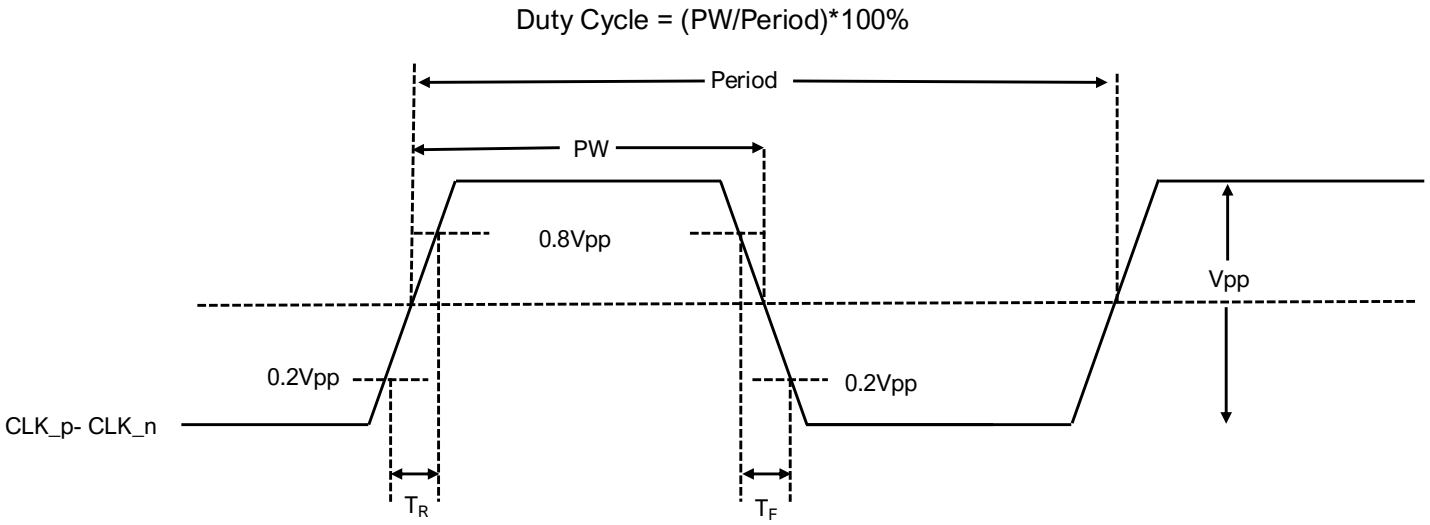


Figure 17. Output Timing across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps

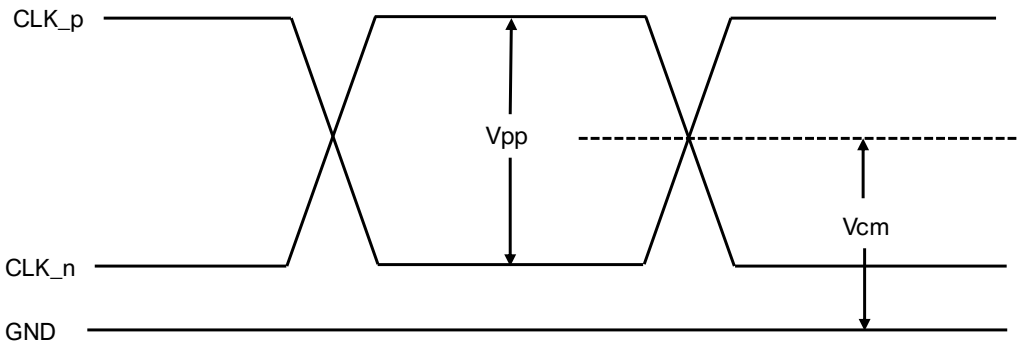


Figure 18. HCSL Output Level across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

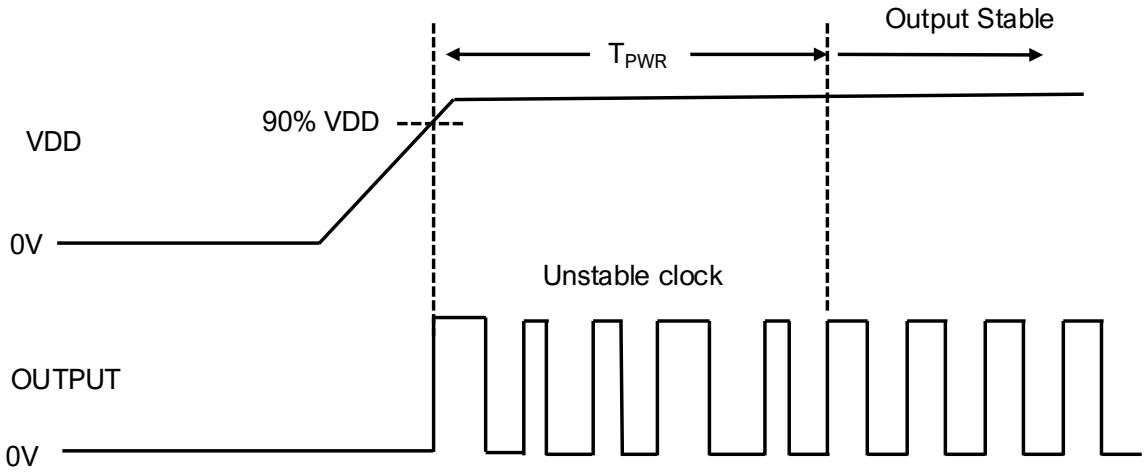


Figure 19. Powerup Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

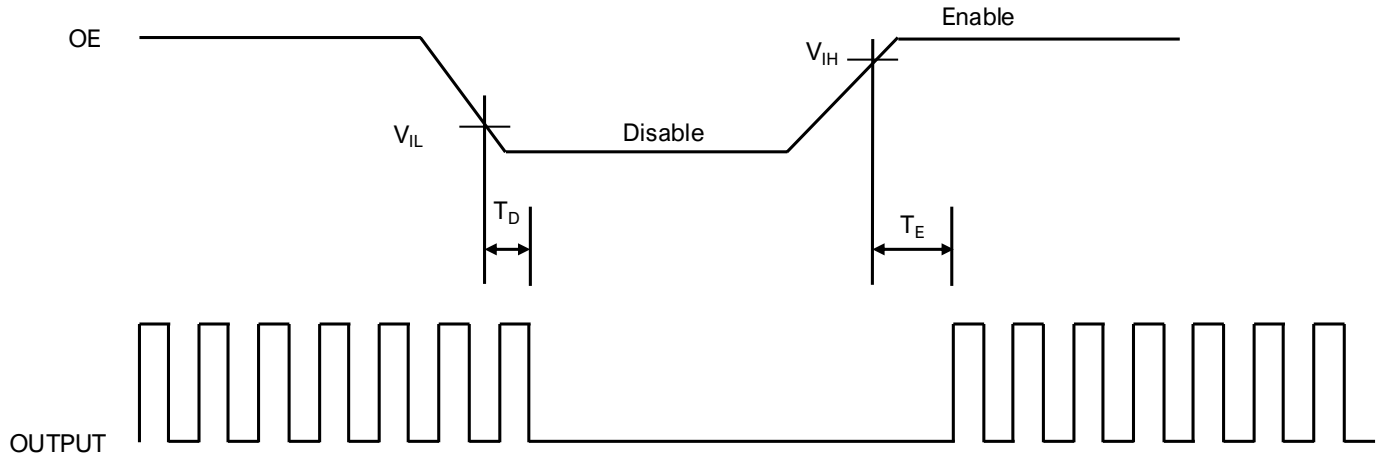


Figure 20. OE Enable/Disable Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs

Packaging Information

Figure 21 shows the MS2008 packaging drawing.

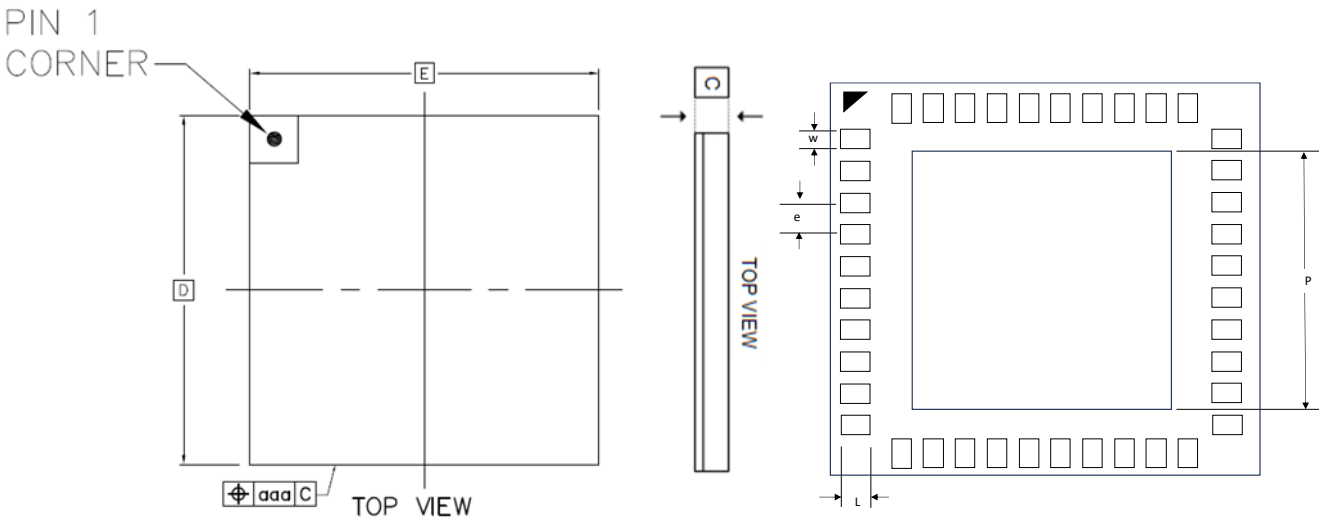


Figure 21. MS2008 Packaging Drawing (5X5, 40LGA)

Table 9. Package Dimensions

	SYMBOL	MIN	NOM	MAX
Total Thickness	C	0.896	0.946	0.996
Body Size	D		5 BSC	
	E		5 BSC	
Exposed Pad	P	3.5	3.6	3.7
Lead Pitch	e		0.4 BSC	
Lead Width	W	0.15	0.20	0.25
Lead Length	L	0.30	0.40	0.50
Package Edge Tolerance			0.1	
Mold Flatness			0.2	
Coplanarity			0.08	

Packaging Land Pattern

Figure 22 shows the MS2008 PCB land pattern.

Note: All dimensions are in millimeters

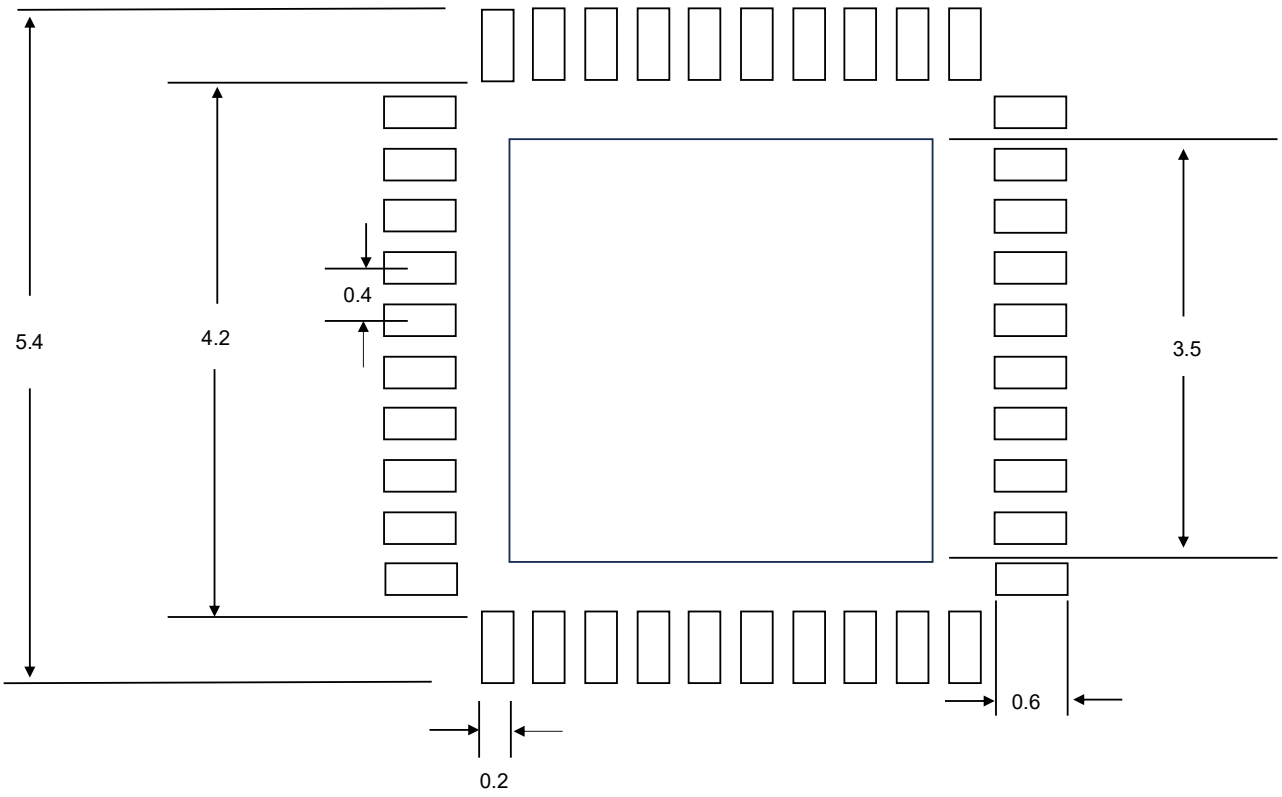


Figure 22. MS2008 Packaging Land Pattern Drawing (5X5, 40LGA)

Device Top Marking

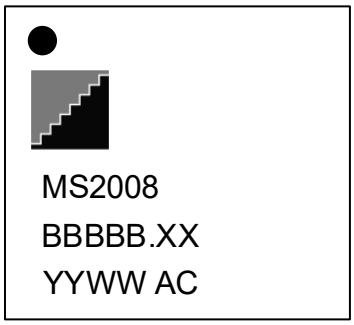


Figure 23. MS2008 Device Top Marking Showing Pin 1

Table 10. MS2008 Device Marking Legend

Line	Position	Description
1	1	Pin 1 Orientation Mark (Dot)
2	1	Mixed-Signal Logo
3	1-6	Product Marking
4	1-5	Wafer Lot Number
	6-7	Wafer #
5	Lot Trace Code	
	1-2	Year (last two digits of the year)
	3-4	Calendar Work Week Number (1-53)
	5-6	Assembly Code

Reflow Profile (IPC/JEDEC-STD-020)

Figure 24 shows the reflow profile for MS2008

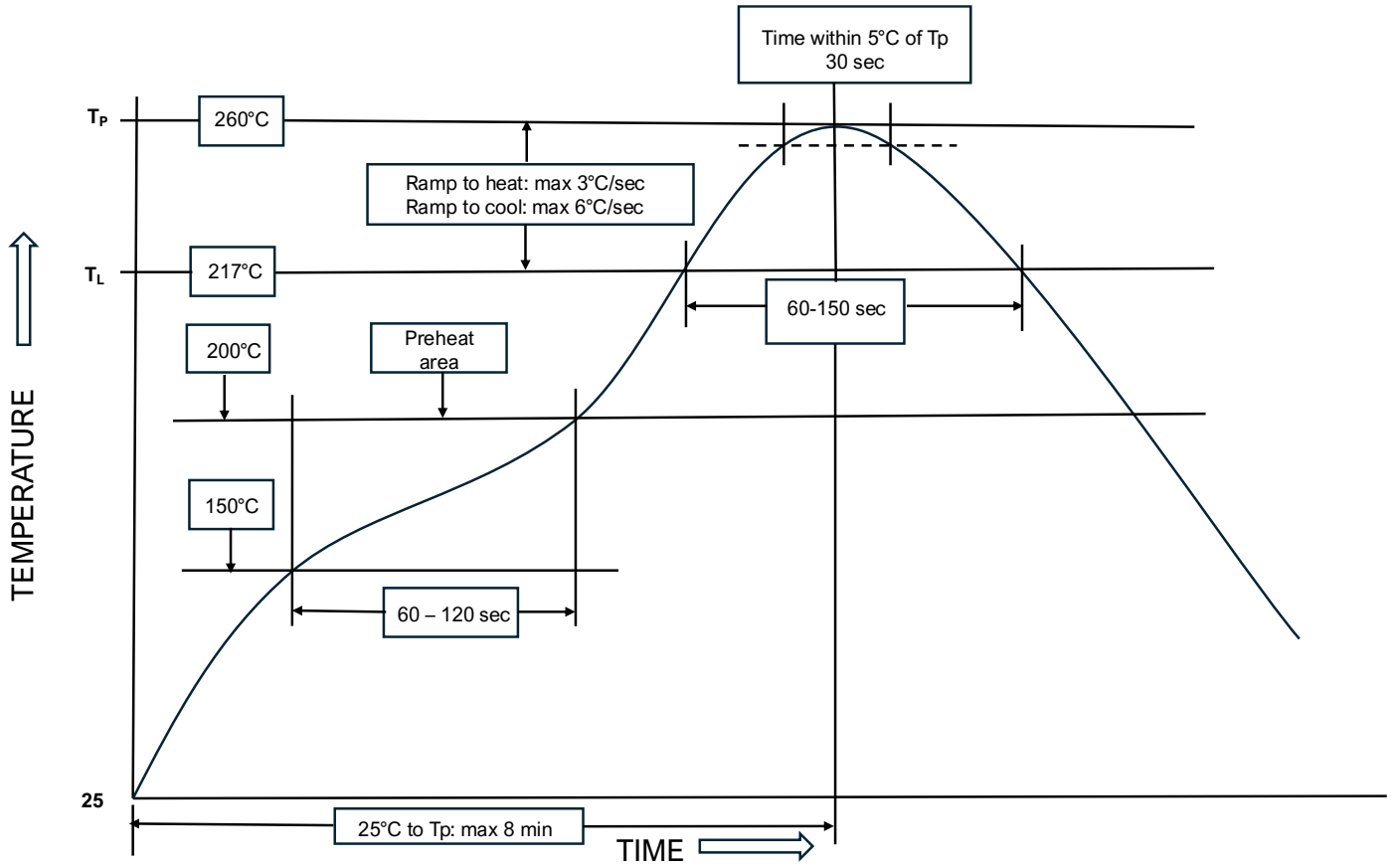


Figure 24. MS2008 Reflow Profile

IMPORTANT NOTICE AND DISCLAIMER

MIXED-SIGNAL DEVICES INC. PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

Mailing Address: Mixed-Signal Devices Inc, 2 Venture, Suite 300, Irvine, California 92618, USA Copyright © 2026.