Preliminary Data Sheet

MS1220

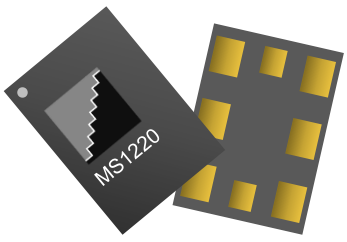
Ultra-Low Jitter Voltage Controlled Oscillators (VCO)

Features

- Available at any frequency from 10 MHz to 1000 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 34.9 fs at 156.25 MHz
  - 24.6 fs at 312.50 MHz
  - 26.1 fs at 491.52 MHz
  - 26.8 fs at 625 MHz
- Total stability of ±1 ppm
- Programmable tuning slope (Kvco) up to 300 ppm/V
- CML/LVDS/LVDS-EXT/LVPECL/HCSL output formats
- Simplified BoM with no external loop filters
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Industry standard 3.2X2.5 mm 8-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- SONET/SDH
- 10 GbE LAN/WAN
- Wireless Infrastructure
- Synchronous Ethernet
- Optical modules
- Clock and data recovery
- Clock Generation and Frequency Translation
- High-performance replacement for SAW



General Description

MS1220 is a digitally synthesized voltage-controlled oscillator (VCO) that combines advanced Bulk Acoustic Wave (BAW) resonator technology with high-performance digital frequency synthesis to deliver highly stable, fully programmable multi-GHz clocks with extremely low phase Jitter.

Built-in Adaptive Intelligence continuously monitors operating conditions in the background, using autonomous DSP algorithms to maintain robust and consistent performance across process, voltage, and temperature.

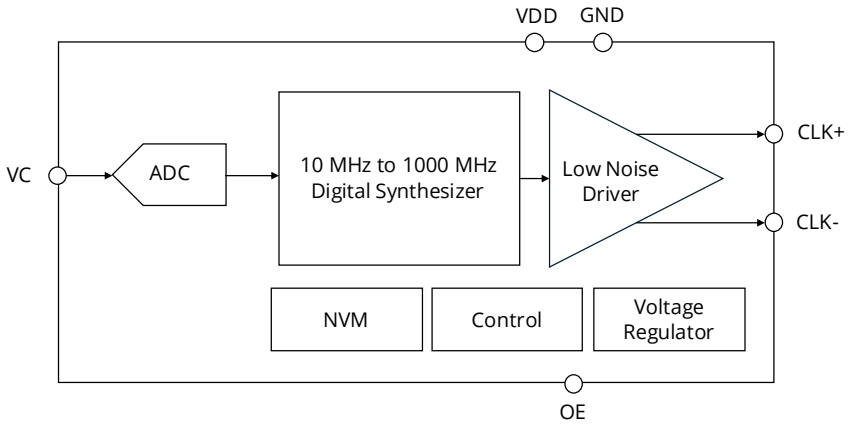
The devices are factory programmed to provide an accurate frequency between 10 MHz and 1000 MHz at less than 1 ppb resolution.

The MS1220 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

Device Information

Part Number	Package	Description
MS1220	3.2X2.5 mm 8-pin LGA	VCO

Figure 1. Functional Block Diagram



Pin Assignment and Pin Description

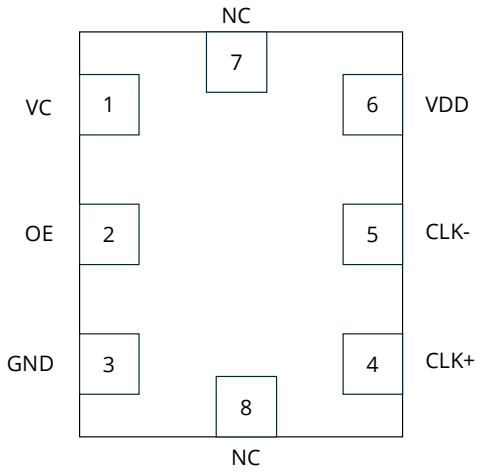


Figure 2. MS1220 Pin Assignments

Table 1. MS1220 Pin Descriptions

Pin No	Name	Description
1	VC	Control Voltage
2	OE	Output Enable • High/Floating: Output enabled (Internal pull-up of 100kΩ) • Low: Output disabled
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply – connect bypass capacitor between this pin and pin 3. Keep bypass as close as possible to the pins
7	NC	No Connect
8	NC	No Connect

Part Ordering Information

Figure 3 shows a logic tree for ordering each of the three available parts.

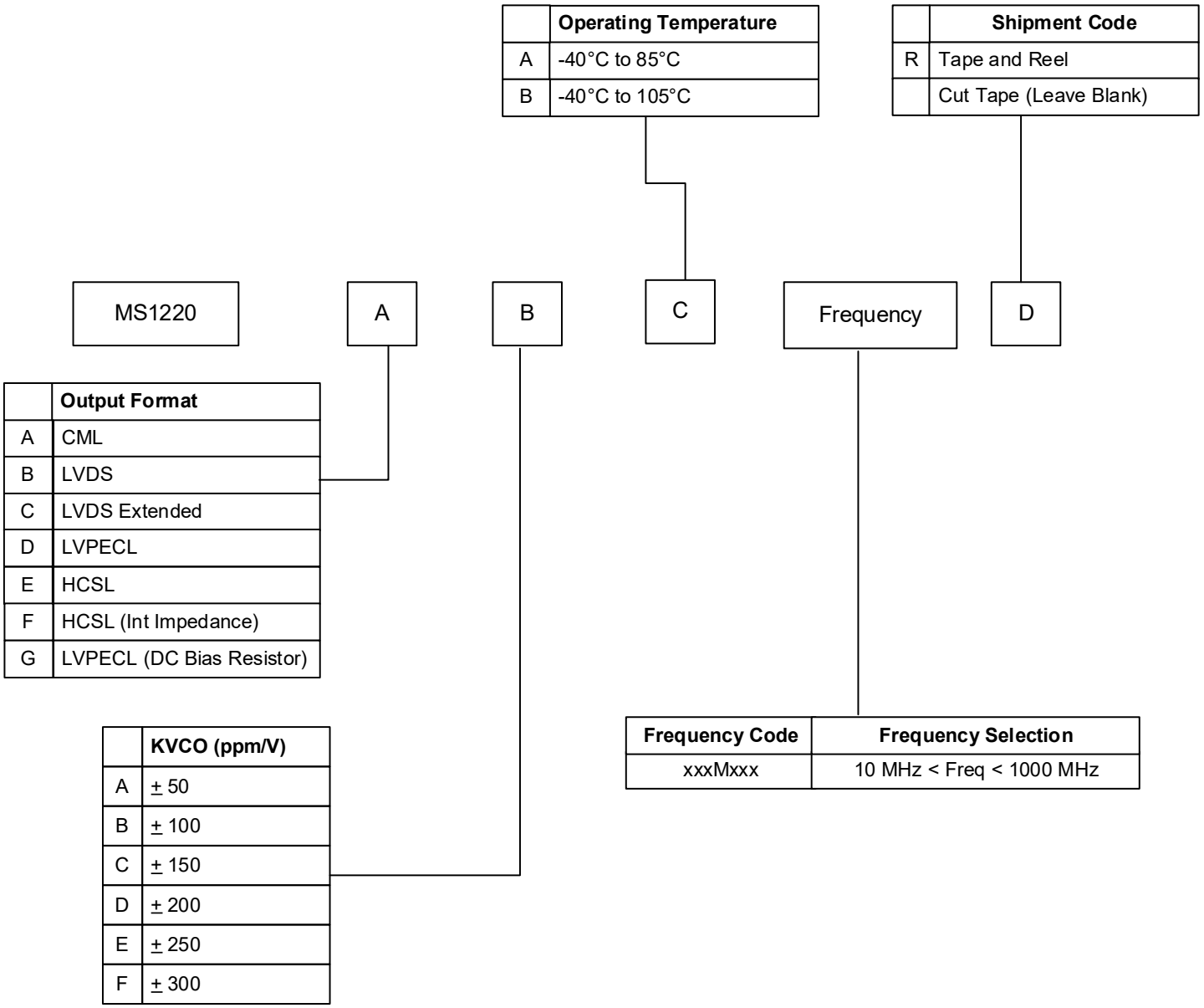


Figure 3. MS1220 Part Ordering Information

Table 11. Example of ordering part number

Base P/N	Output Format	KVCO (ppm/V)	Operating Temperature	Frequency Code	Shipment Type	**Ordering part number**
MS1220	LVDS	±150	-40°C to 85°C	312.5 MHz	Tape and Reel	**MS1220BCA312M500R**
MS1220	LVPECL	±50	-40°C to 105°C	625 MHz	Tape and Reel	**MS1220DAB625M000R**

Specifications

Table 2. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination. A 0.1uF and 10uf bypass capacitor should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Frequency Range	F_{CLK}	All Output Formats	10		1000	MHz
Frequency Stability						
Frequency Stability (Temperature)	F_{TS}	-40°C to 105°C	-1		1	ppm
Frequency Tolerance	F_{INIT}	25°C±2°C, after 2x flow soldering	-1		+1	ppm
First Year Aging	F_1yr	25°C±2°C	-1		1	ppm
Clock Output Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz)	Φ_{JITTER}	Frequency=312.5 MHz		24.6	37	fs
		Frequency=625 MHz		26.8	40	fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		1.71	1.8	1.89	V
Temperature Range	T_A	Industrial Temperature	-40		85	°C
		Extended Industrial Temperature	-40		105	°C

Current Consumption

Supply Current	I_{DD}	LVDS Output (Output Enabled)		80	100	mA
		All Other Outputs (Output Enabled)		90	110	mA
		Tristate Hi-Z (Output Disabled)		50	60	mA

Input Characteristics

Digital Input Levels (OE)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	Us
	T_E	Output Enable Time			20	Us
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	Ms

PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (312.5MHz)		-114		dBc
Power Supply-Jitter Sensitivity	PSJS			0.1		fs/mv

Note:

(1) Measured with 50 mVpp ripple from 50 KHz to 1 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		50	70	ps
CML Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 9, Figure 10	0.6	0.8	1	V
LVDS Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 11	0.5	0.7	0.9	V
LVDS-EXT Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 11	0.8	1.2	1.6	V
LVPECL Output (AC-Coupled)	Vpp	Differential Pk-Pk See Figure 12, Figure 13	1.2	1.4	1.6	V
HCSL Output (AC or DC-Coupled)	Vpp	Differential Pk-Pk See Figure 14, Figure 15	1.1	1.35	1.6	V
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

Vc Control Voltage Input

Parameter	Symbol	Test Condition/Comment	Min		Typ	Max	Unit
Control Voltage Tuning Slope1	Kvco	0.1V to 0.9V			50		ppm/V
					100		
					150		
					200		
					250		
					300		
Control Voltage Linearity	Lvc	Best Straight Line Fit	-1.5		±0.5	+1.5	%
		KVCO Variation	-10		±5	+10	%
Modulation Bandwidth	BW				10		kHz
Vc Input Impedance	Zvc		500				kΩ
Nominal Control Voltage	Vcnom	@fo			0.5		V
Control Voltage Tuning Range	Vc		0.1			0.9	V

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C

Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.

Table 4. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
3.2mmX2.5mm 8 pin LGA	Thermal Resistance, Junction to Ambient	$ø_{JA}$	80	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C

Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.

Table 5. Environmental Compliance

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Moisture Sensitivity Level (MSL)	3
Note: For additional information not listed, please contact Mixed-Signal Devices.	

Table 6. ESD Levels

Description	Description	Specification	Level
HBM[1]	Human Body Model	JEDEC JS-001	2000V
CDM[2]	Charge Device Model	JEDEC JESD22-C101	500V

Notes:
1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155
2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157

Table 7. Typical Output Phase Noise Characteristics
VDD= 1.8V, T_A = 25°C, Output Type = LVDS-EXT

Offset frequency	156.25 MHz	312.50 MHz	491.52 MHz	625 MHz	Unit
1 KHz	-106	-103	-100	-98	dBc/Hz
10 KHz	-138	-133	-128	-127	dBc/Hz
100 KHz	-157	-154	-149	-147	dBc/Hz
1 MHz	-167	-163	-158	-156	dBc/Hz
10 MHz	-168	-164	-160	-148	dBc/Hz
20 MHz	-168	-164	-159	-158	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	35	25	26	27	fs

Typical Output Measured Phase Noise Plots

This section shows three MS1220 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent 5052B Signal Source Analyzer.

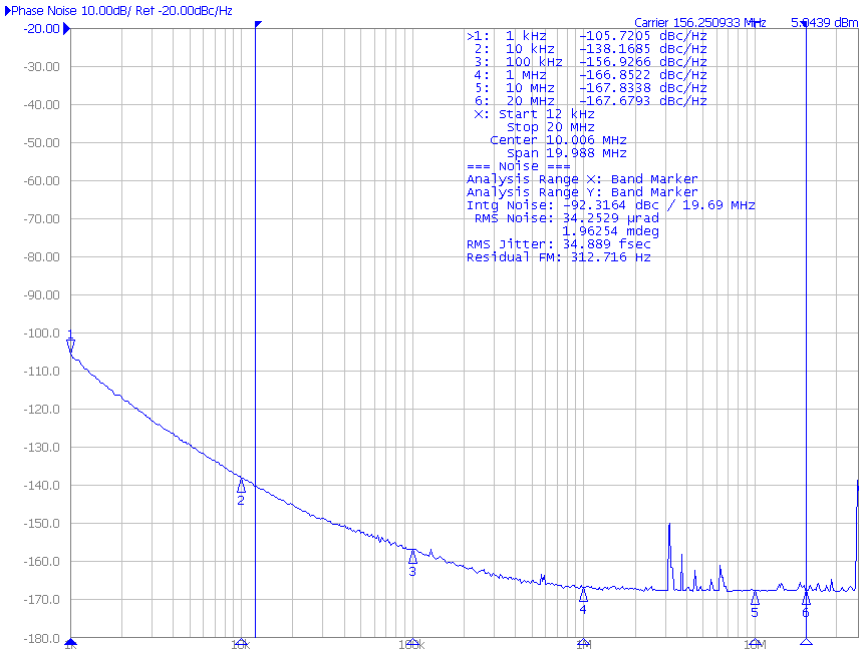


Figure 4. Center Frequency: 156.25 MHz

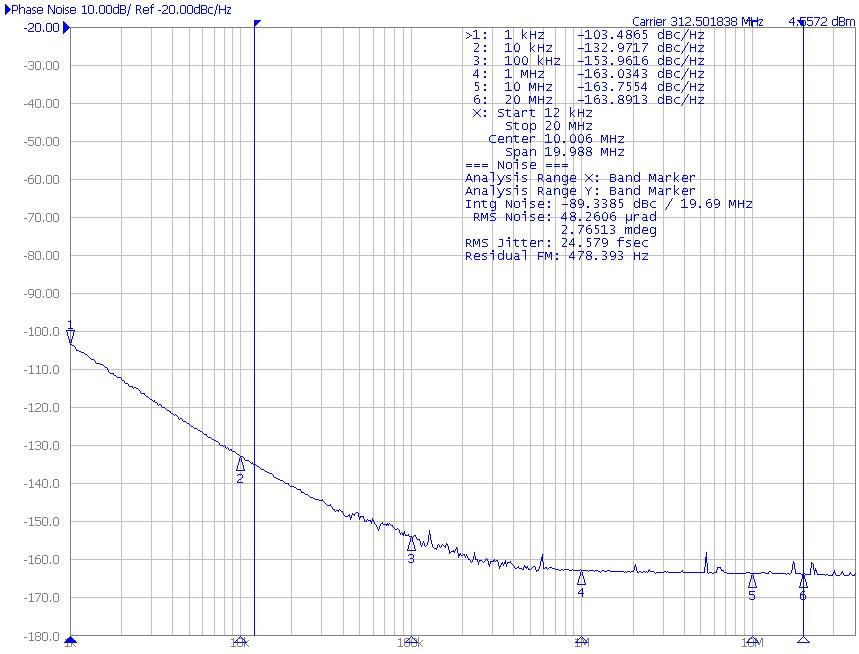


Figure 5. Center Frequency: 312.5 MHz

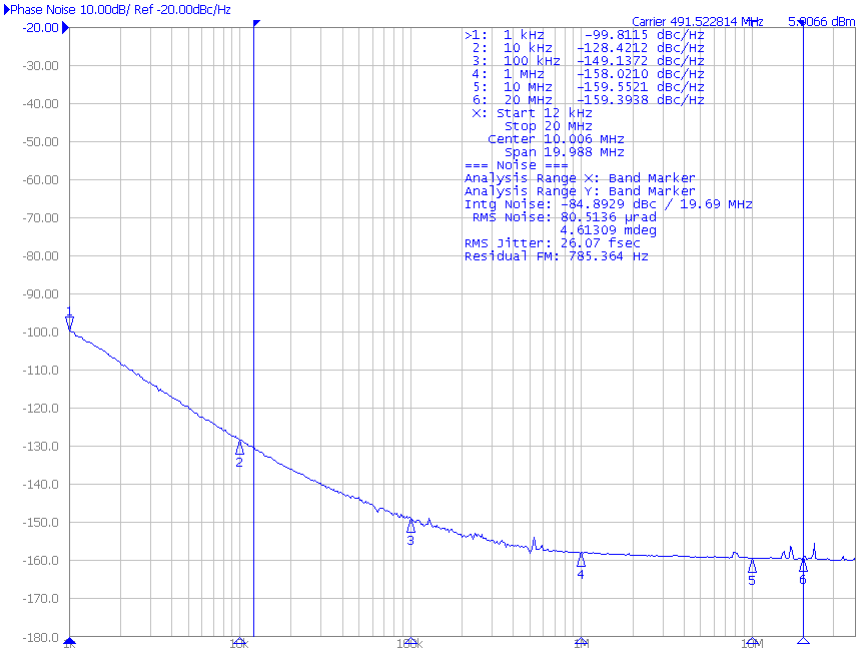


Figure 6. Center Frequency: 491.52 MHz

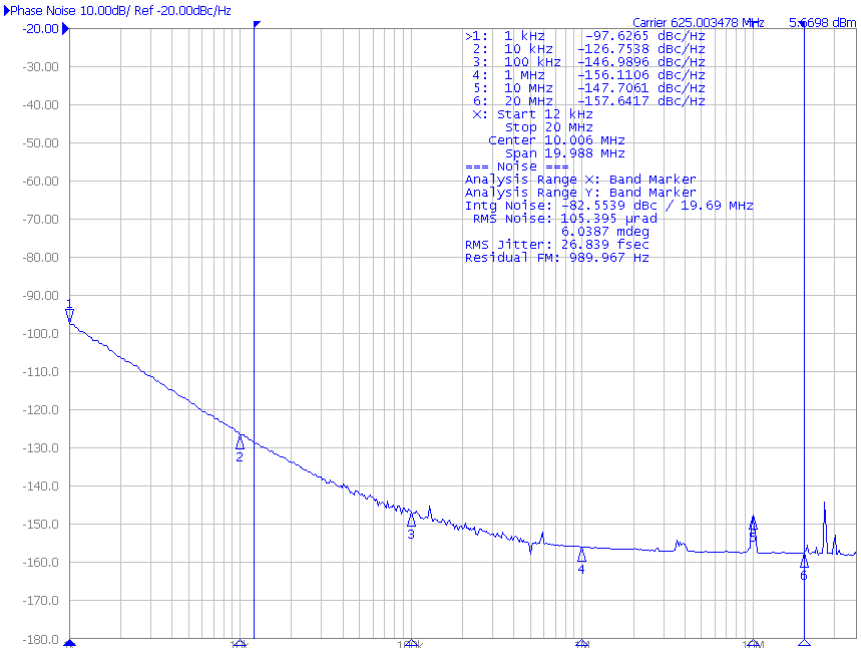


Figure 7. Center Frequency: 625 MHz

Output Terminations

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff
LVDS	0.7V	AC	100 Ω diff
LVDS-EXT	1.2V	AC	100 Ω diff
LVPECL	1.4V	AC	50 Ω to VT
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT
HCSL (Int Term)	1.35V	AC or DC	None
HCSL	1.35V	DC	50 Ω to GND

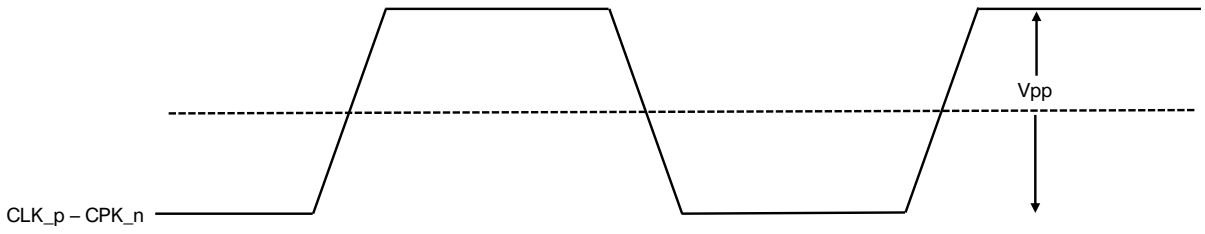


Figure 8. Differential Output Swing

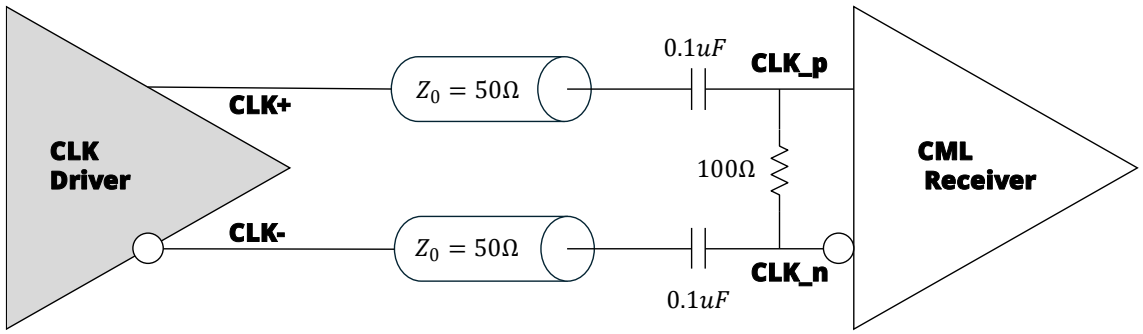


Figure 9. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

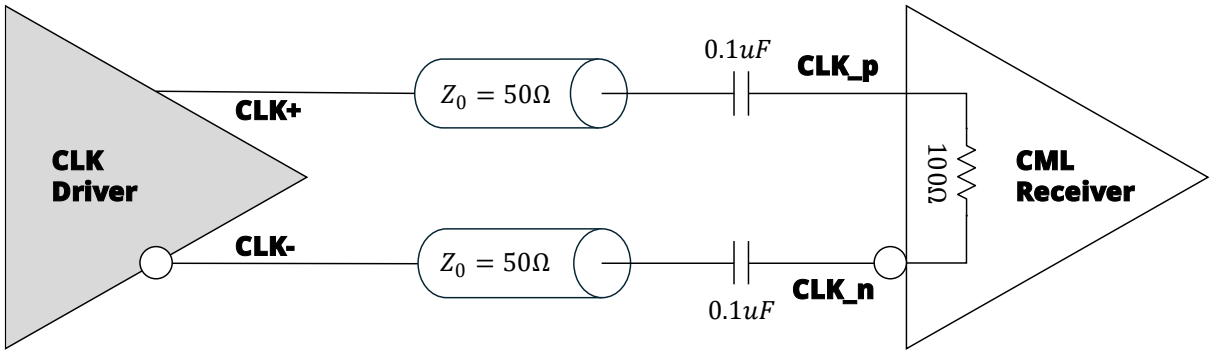


Figure 10. CML Output Driver with 100 Ω Differential Receiver Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
CML	0.8V	AC	100 Ω diff

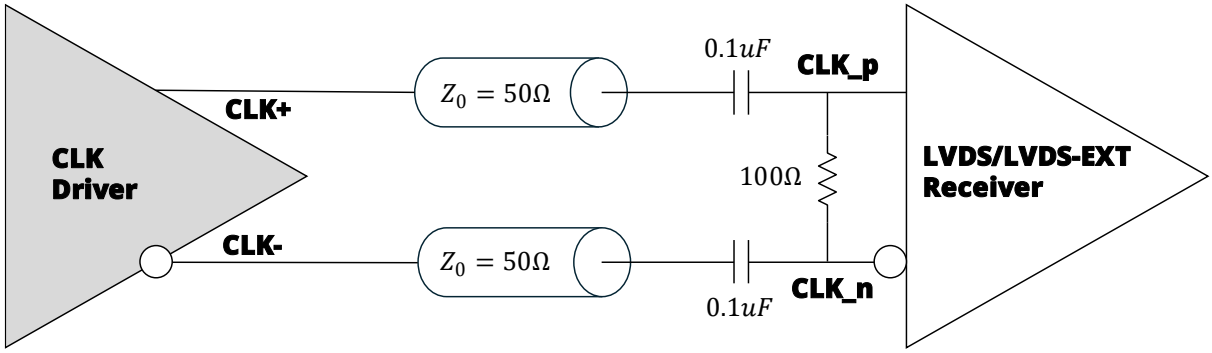


Figure 11. LVDS/LVDS-EXT Output Driver with 100 Ω Differential Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVDS/LVDS-EXT	0.7V/1.2V	AC	100 Ω diff

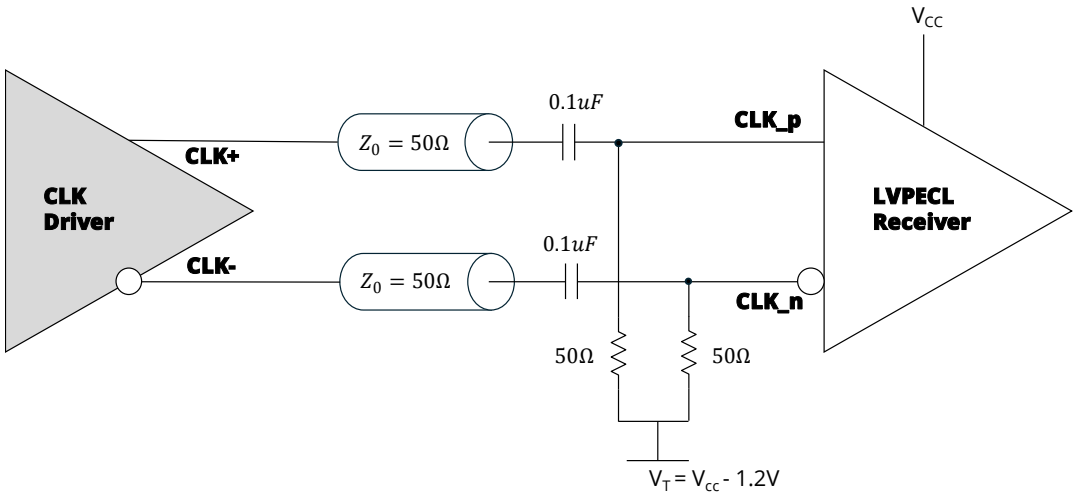


Figure 12. LVPECL Output Driver with External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL	1.4V	AC	50Ω to VT

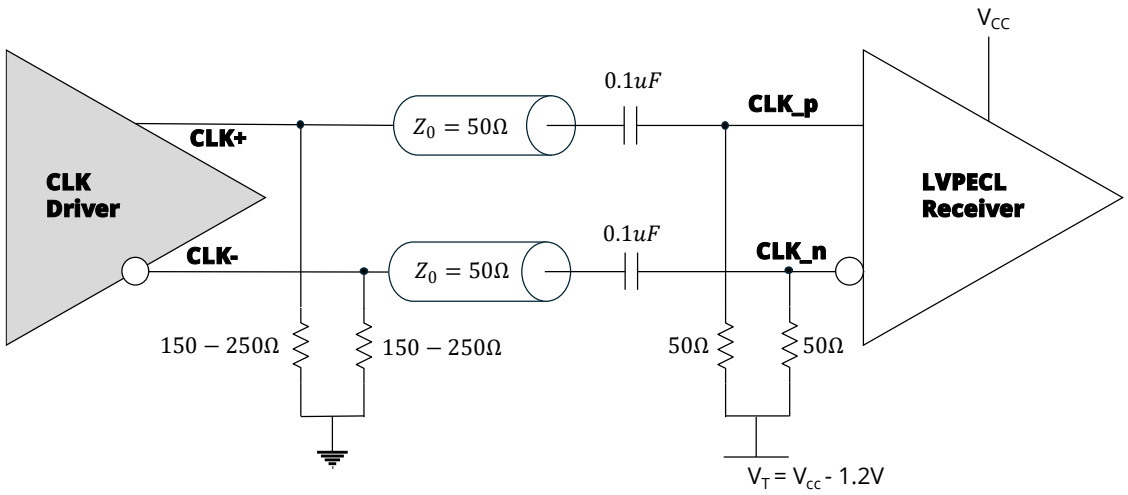


Figure 13. LVPECL Output Driver with Source Bias Resistors and External VT Bias Termination

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
LVPECL (DC Bias Resistor)	1.4V	AC	150 Ω to 250 Ω to GND, 50 Ω to VT

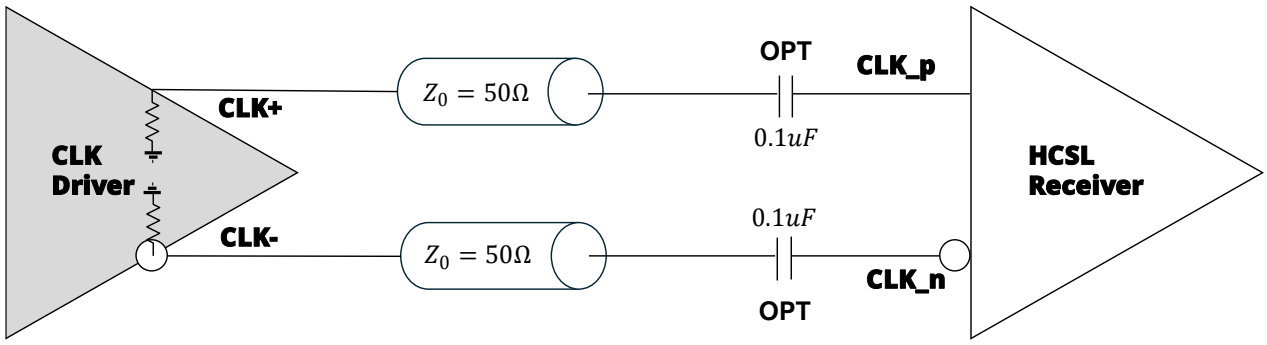


Figure 14. HCSL Output Driver with Integrated Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL (Int Term)	1.35V	AC/DC	None

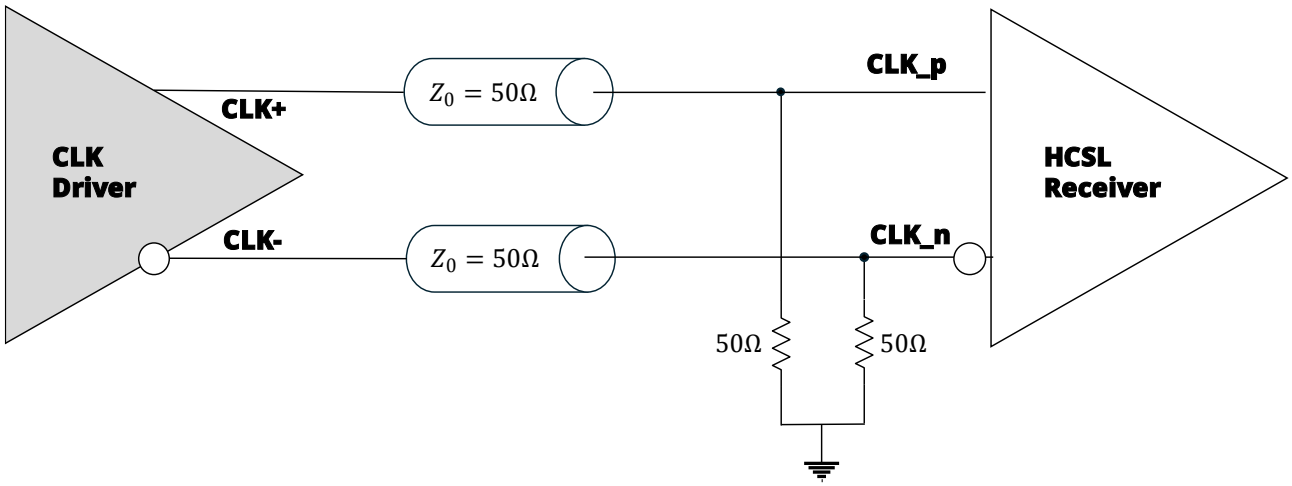


Figure 15. HCSL Output Driver with 50 Ω Receiver Termination to Ground

Output Type	Differential Output Swing Vpp (Typ)	Coupling	Termination
HCSL	1.35V	DC	50 Ω to GND

Output Timing

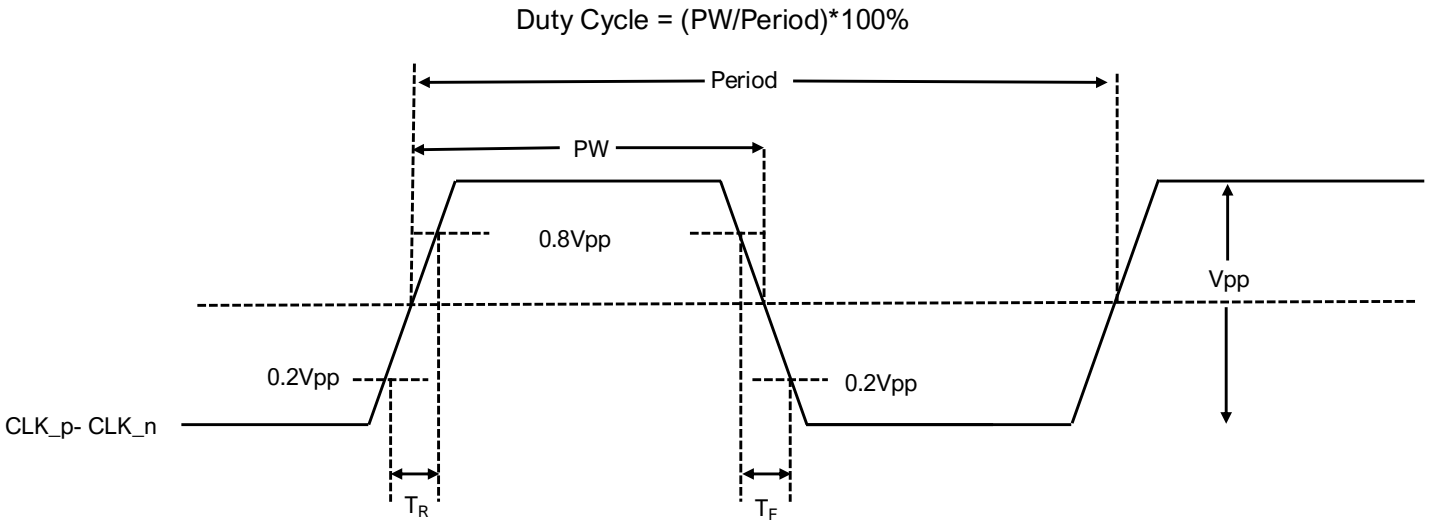


Figure 16. Output Timing across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		60	80	ps

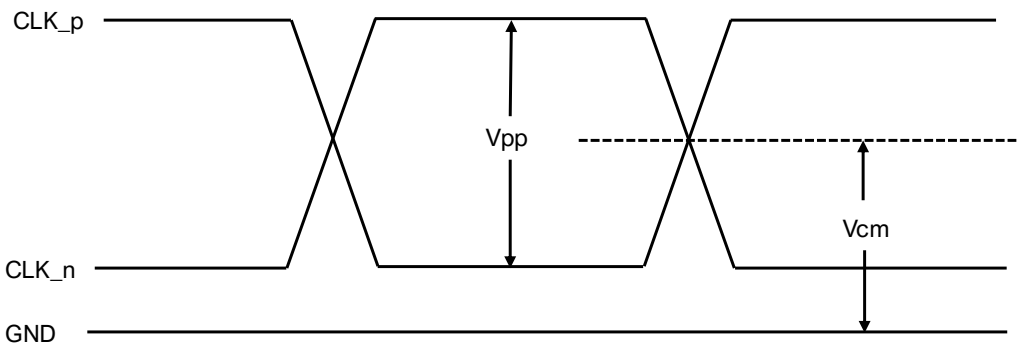


Figure 17. HCSL Output Level across differential pair (CLK_p - CLK_n)

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
HCSL Output Voltage (DC- Coupled)	V_{CM}	Common Mode Voltage	340	350	360	mV

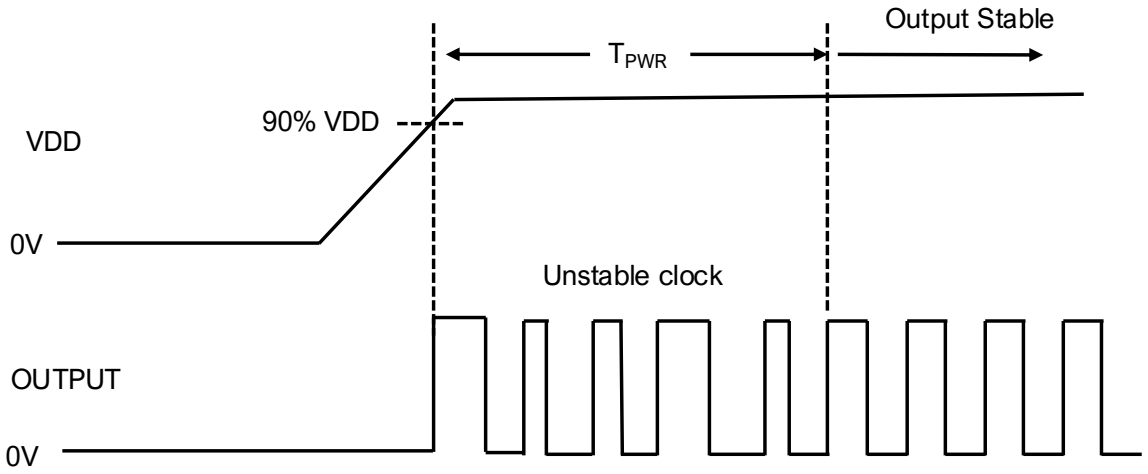


Figure 18. Powerup Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

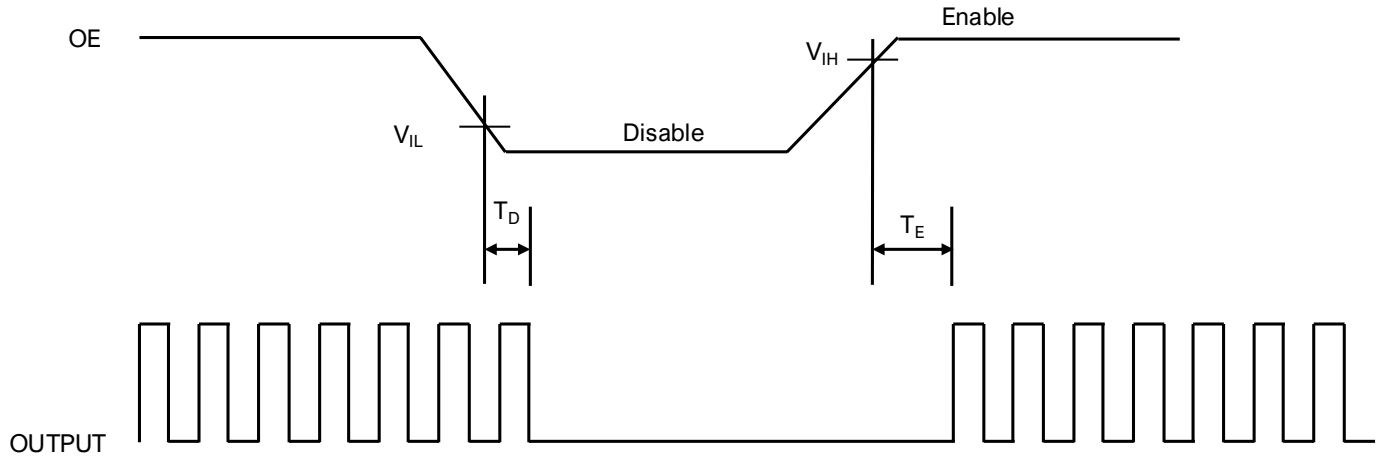


Figure 19. OE Enable/Disable Timing

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Output Enable (OE)	T_D	Output Disable Time			3	µs
	T_E	Output Enable Time			20	µs

Packaging Information

Figure 20 shows the MS1220 packaging drawing.

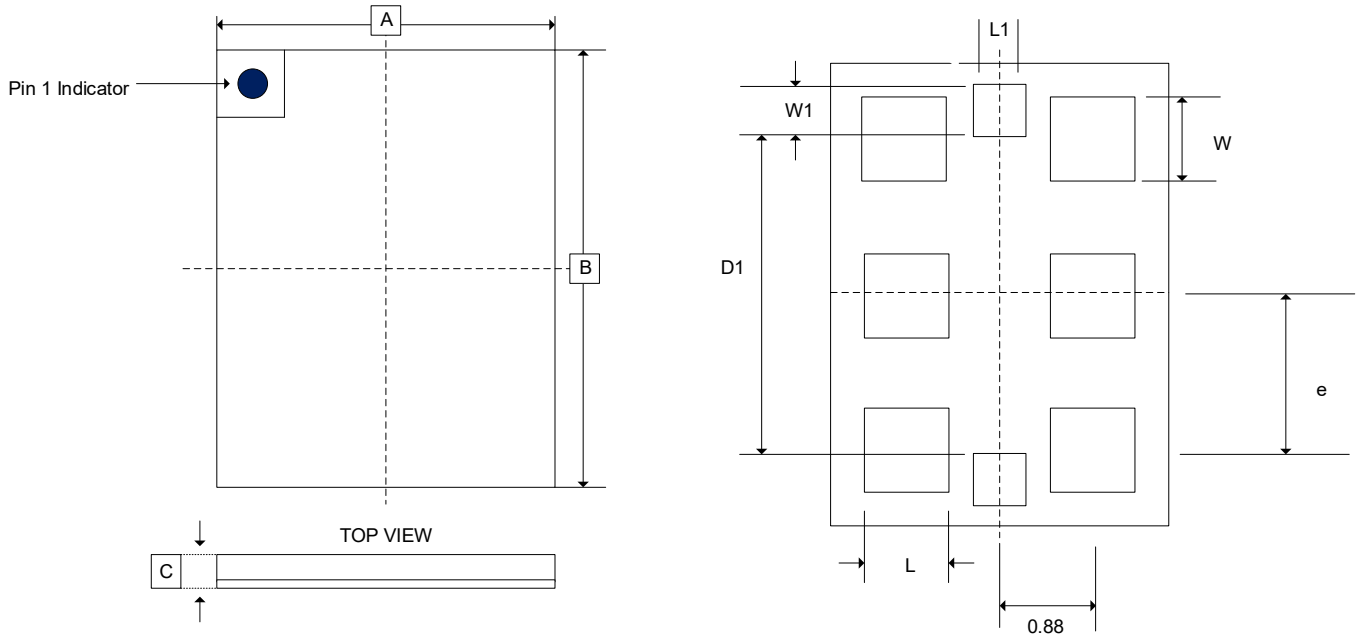


Figure 20. MS1220 Packaging Drawing (3.2mm x 2.5 mm)

Table 8. MS1220 Packaging Dimensions

Dimensions	Min	Nom	Max
A		2.5 BSC	
B		3.2 BSC	
C	1.246	1.346	1.446
W	0.55	0.6	0.65
L	0.5	0.55	0.6
W1	0.35	0.4	0.45
L1	0.35	0.4	0.45
e		1.1 BSC	
D1		2.2 BSC	
Package Edge Tolerance		0.1	
Mold Flatness		0.1	
Coplanarity		0.08	

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 21 shows the MS1220 PCB land pattern.

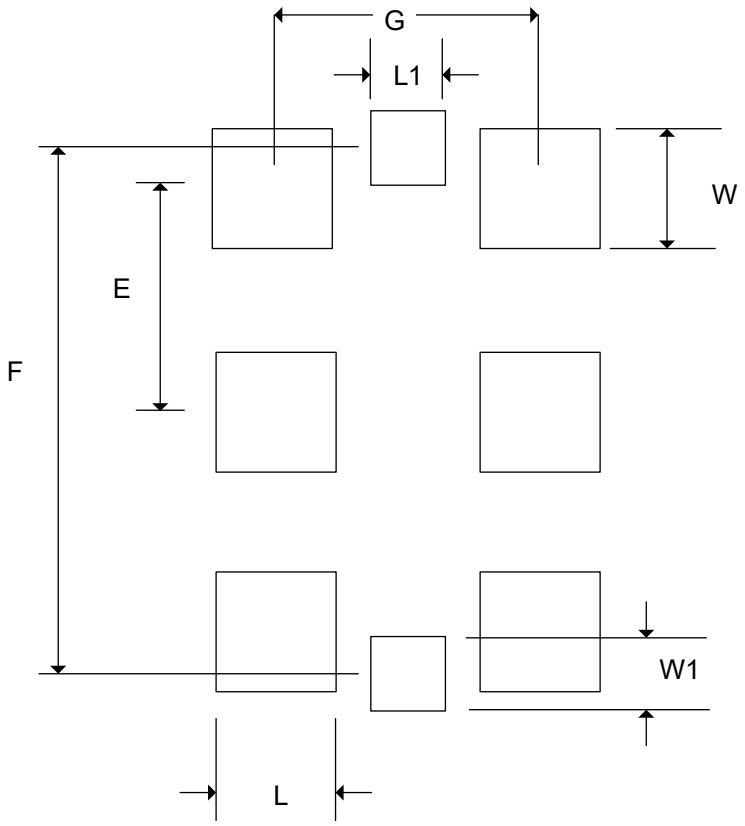


Figure 21. MS1220 Packaging Land Pattern Drawing (3.2mm x 2.5mm)

Table 9. MS1220 Packaging Land Pattern Dimensions

Dimensions	In mm
L	0.7
W	0.7
L1	0.5
W1	0.55
E	1.1
F	2.6
G	1.76

Device Top Marking

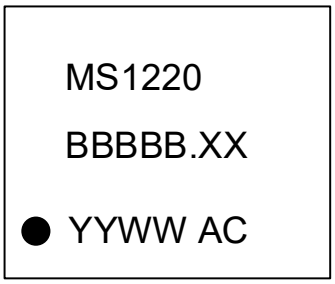


Figure 22. MS1220 Device Top Marking Showing Pin 1

Table 10. MS1220 Device Marking Legend

Line	Position	Description
1	1	Part Number
2	1-5	Wafer Lot Number
	6-7	Wafer #
3	Lot Traceability	
	1	Pin 1 Orientation Mark (Dot),
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	6-7	Assembly Code

Reflow Profile (IPC/JEDEC-STD-020)

Figure 23 shows the reflow profile for MS1220

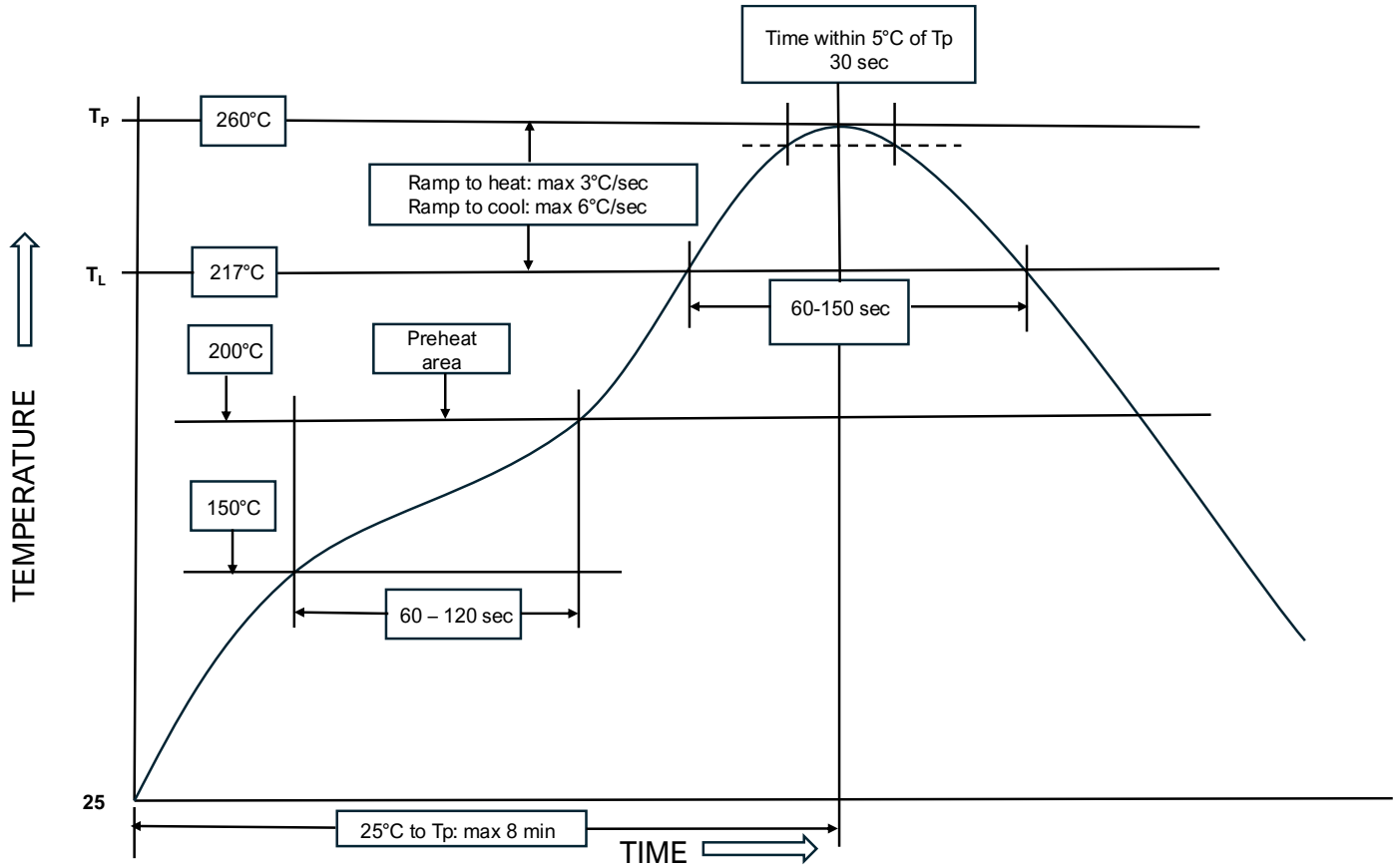


Figure 23. MS1220 Reflow Profile

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