

MIXED SIGNAL DEVICES INC.

MS11XX

Digital Synthesized Oscillator

Reference Design Guide

Revision 1.0 | July 2026

1. Overview

This reference design guide provides hardware engineers with recommended circuit implementations, layout guidance, and best application practices for the Digital Synthesized Oscillator. The MS11xx are MSDI's flagship Digital Synthesized Oscillator (DSO) product, offering ultra-low phase noise, a configurable differential output driver (CML, HCSL, LVPECL, LVDS, and Extended LVDS), and exceptional frequency stability across temperature—targeting data center, fiber optic module, and high-reliability telecom applications.

1.1 Product Highlights

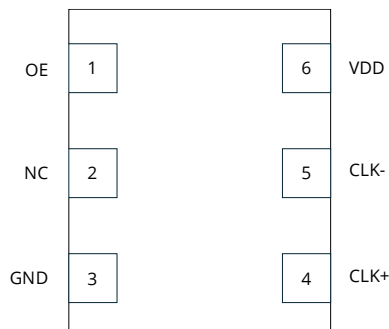
Parameter	MS115x/MS119x Specification
Frequency Range	20 MHz – 2200 MHz
Frequency Stability	±20 ppm
RMS Phase Jitter (12 KHz – 20 MHz)	20 fs (Frequency = 625 MHz)
Output Format	LVDS, LVDS-EXT, CML, HCSL, LVPECL
Supply Voltage	1.8 V
Package	2.5 X2.0 mm, 2.0X1.6 mm, 6L
Operating Temperature	–40°C to +85°C (Industrial); –40°C to +105°C (Extended Range)
Enable/Disable (OE)	Active-high, tri-state output when OE = Low

Parameter	MS113x/MS118x Specification
Frequency Range	10 MHz – 1000 MHz
Frequency Stability	±20 ppm
RMS Phase Jitter (12 KHz – 20 MHz)	25 fs (Frequency = 312.5 MHz)
Output Format	LVDS, LVDS-EXT, CML, HCSL, LVPECL
Supply Voltage	1.8 V, 2.5 V/3.3 V (MS1135)
Package	2.5 X2.0 mm, 2.0X1.6 mm, 6L
Operating Temperature	–40°C to +85°C (Industrial); –40°C to +105°C (Extended Range)
Enable/Disable (OE)	Active-high, tri-state output when OE = Low

2. Pin Configuration and Description

2.1 6-Pad LGA Package

Figure 2-1 shows the top-view pinout.

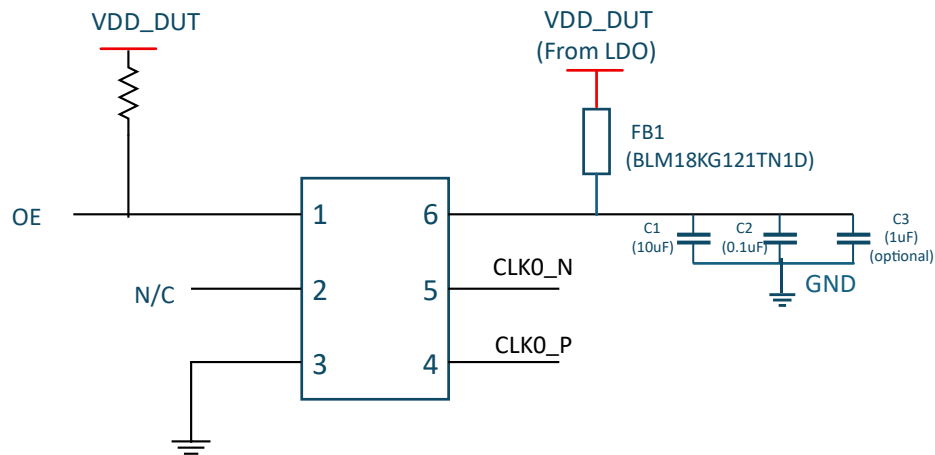


[Figure 2-1: Package Pad Layout – 2.5X2.0 mm, 2.0X1.6mm, 6-Pad SMD]

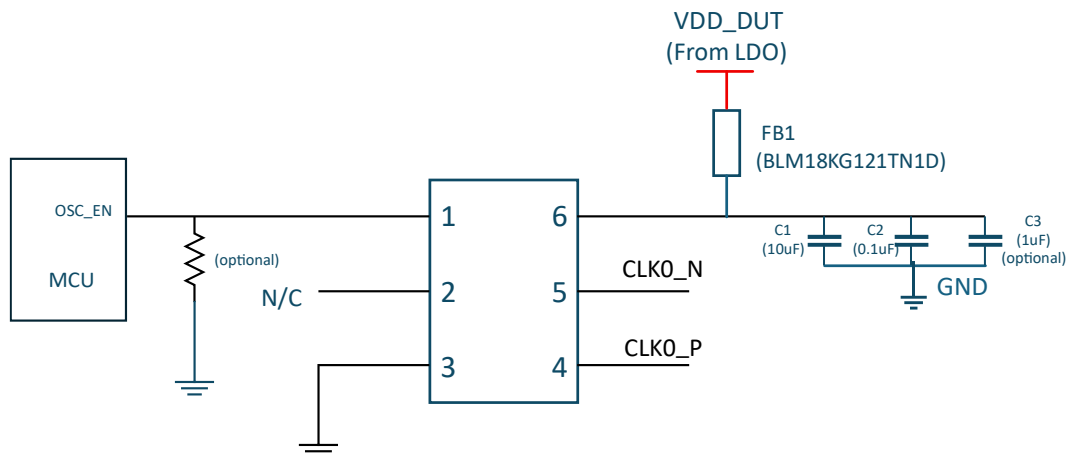
Pad #	Name	Description
1	OE	Output Enable High/Floating: Output enabled (Internal pull-up of 100kΩ) Low: Output disabled
2	NC	No Connect – leave floating
3	CLK+	Clock output
4	CLK–	Complementary clock output
5	VDD	Power supply
6	GND	Ground

3. Recommended Application Circuits

Case 1: Oscillator OE tied to VDD

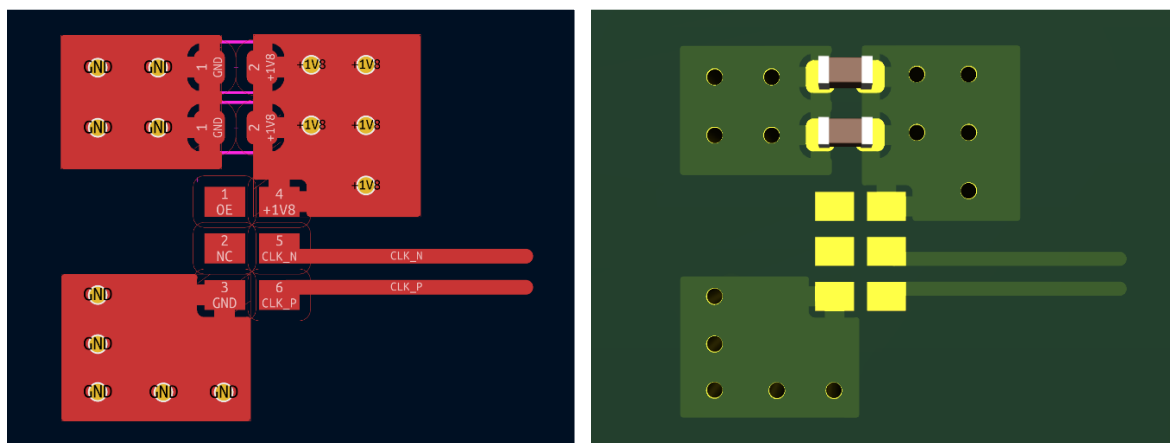


Case 2: Oscillator OE driven by MCU



4. Power Supply Decoupling

The MS11XX is optimized for low phase noise performance. To achieve the best close-in phase noise, use proper power supply decoupling and follow the recommended PCB layout guidelines.



[Figure 4-1: MS11XX Recommended layout]

4.1 Decoupling Strategy

- Place high-frequency decoupling capacitors as close as possible to the device power supply (VDD) pins to minimize supply impedance.
- Include sufficient bulk capacitance near the device to support transient load current and maintain a stable supply voltage.
- Connect decoupling capacitors directly to the VDD pins and the ground plane using short, low-inductance traces and vias.
- For applications requiring the lowest phase noise and jitter, power the device from a clean, low-noise regulator with adequate power supply rejection over the relevant frequency range.
- If a switching regulator is used, minimize coupling of switching noise into the oscillator by keeping power switching circuitry and its routing away from the oscillator and high-speed output signals.

5. PCB Layout Guidelines

To achieve the best phase noise and jitter performance from the MS11XX, follow the recommended PCB layout guidelines below. The recommendations are listed in priority order.

5.1 Ground Plane

- Provide a continuous, uninterrupted ground plane beneath the MS11XX, extending at least two times the package footprint in all directions.
- Avoid routing signal traces on the PCB layer immediately below the ground plane beneath the oscillator to maintain optimum phase noise and jitter performance.

5.2 Output Trace Routing

- Route CLK output as a 50 Ω controlled-impedance microstrip or stripline (dielectric properties per PCB stackup).
- Minimize trace length from CLK output to the first receiver or termination. Target < 10 cm for LVPECL/LVDS with proper termination.
- Avoid 90° bends; use 45° mitered corners or curved routing.
- Maintain $\geq 3\times$ trace-width clearance between the CLK trace and any switching supply, digital bus, or high-speed data lines.
- Do not route CLK traces through or near power supply inductors or ferrite beads.

5.3 Differential Pair Routing (LVPECL / LVDS)

- Route CLK+ and CLK– as a tightly coupled differential pair with ≤ 5 mil intra-pair spacing and $\leq 5\%$ mismatch in trace length (skew budget: < 0.5 ps).
- Maintain pair isolation from single-ended signals: minimum 20 mil clearance.
- Place AC-coupling capacitors symmetrically on both CLK+ and CLK– lines, equidistant from U1.

5.4 Soldering and Assembly

- Recommended reflow profile: peak temperature 245°C max, time above liquidus (217°C) ≤ 60 seconds (IPC/JEDEC J-STD-020)
- Avoid rework with direct hot-air to the oscillator body; use localized rework tools with ESD-safe tip.
- Bottom exposed thermal pad: use solder paste with 50–70% stencil aperture coverage (4 $\times$ via-in-pad or solid paste, depending on reflow process).
- Post-reflow inspection: X-ray verification recommended confirming pad wetting and via fill quality on thermal pad.

6. Output Enable (OE) Pin Operation

The OE pin controls the MS11XX clock output state. When OE is held Low, the CLK output is tri-stated (high impedance) to minimize power consumption and eliminate clock glitches during power-sequencing.

OE Logic Level	Output State	Notes
High ($\geq 0.7 \times VDD$)	Active – Clock running	Normal operation. Typical propagation delay from OE assertion to clock output: $\leq 5 \mu s$.
Low ($\leq 0.3 \times VDD$)	Tri-state (Hi-Z)	Device continues oscillating internally. Re-enable time to valid clock: $\leq 100 \mu s$.
Float / Open	Active – Clock running	Internal Pull-up 100 k Ω resistor

Design Tip: During power-up sequencing, assert OE Low until VDD stabilizes within the recommended operating range, then assert High. This prevents spurious output glitches during supply ramp.

7. Startup and Power Sequencing

The MS11XX requires no external crystal or XTAL reference; the resonator is fully integrated. Upon VDD application:

1. VDD ramp time: 0.1 ms to 10 ms. Faster ramp rates are acceptable; the device is not damaged by instantaneous power application.
2. Internal oscillator startup: Product begins oscillating within 2 ms of VDD reaching minimum operating voltage.
3. Frequency settling: output frequency is within ± 1 ppm of final value within 10 ms of startup.
4. OE can be asserted (High) at any point after VDD is stable. For clean startup, assert OE after 10 ms to ensure settled output.

8. Revision History

Rev	Date	Description
1.0	July 2026	Initial release.

Legal Notice & Disclaimer

Information in this document is provided in connection with Mixed Signal Devices Inc. (MSDI) products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. MSDI reserves the right to make changes to specifications and product descriptions at any time, without notice. MSDI products are not designed, intended, or authorized for use in applications where failure could result in injury, death, or significant property damage. Contact MSDI applications engineering before using MSDI products in such applications.

© 2026 Mixed Signal Devices Inc. All rights reserved. MS11XX is a trademark of Mixed Signal Devices Inc. All other trademarks are the property of their respective owners.