

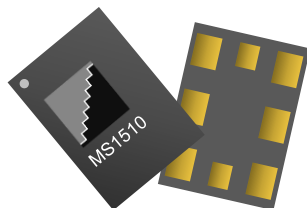
Ultra-High Performance Jitter Attenuator (JA) and Frequency Multiplier (Fx)

Features

- Input frequency from 1 MHz to 750 MHz, gapped clock
- Output frequency from 20 MHz to 2200 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
 - 21.8 fs at 312.50 MHz
 - 21.6 fs at 491.52 MHz
 - 19.6 fs at 625 MHz
 - 21.3 fs at 1250 MHz
 - 18.8 fs at 1600 MHz
- CML/LVDS/LVDS-EXT/LVPECL/HCSL output formats
- Output Enable/Disable Feature
- < 10 ms start-up time
- 3.2X2.5 mm 8-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- SATA
- 10 GbE LAN/WAN
- SAS
- Fiber Channel
- Clock and data recovery
- PCI-Express
- Instrumentation



General Description

The MS1510 combines jitter attenuation and frequency multiplication in a single device. It is powered by our Virtual Crystal™ technology that enables ultra stable fully programmable multi-GHz clocks with extremely low phase noise.

Adaptive fully autonomous DSP algorithms running in the background continuously monitor and ensure robust and consistent performance over process, voltage, and temperature variations.

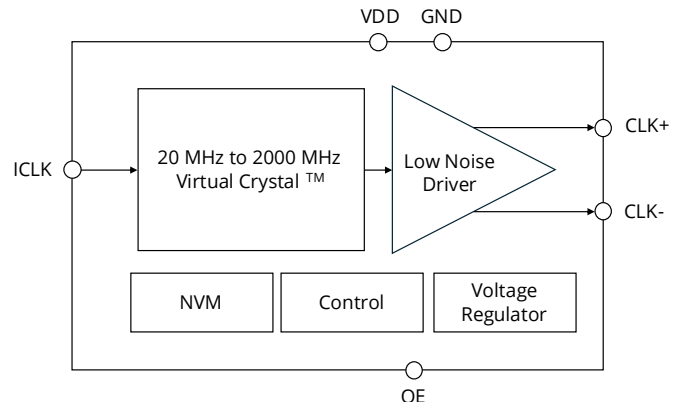
The product can take any input frequency from 1 MHz to 750 MHz and generate any output frequency from 20 MHz to 2200 MHz with <1ppb. The output frequency is synchronized to the input clock. The product is configured using factory programmed NVM.

The MS1510 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

Device Information

Part Number	Package	Description
MS1510	3.2X2.5 mm 8-pin LGA	Jitter Attenuator Frequency Multiplier

Figure 1. Functional Block Diagram



MS1510

Pin Assignment and Pin Description

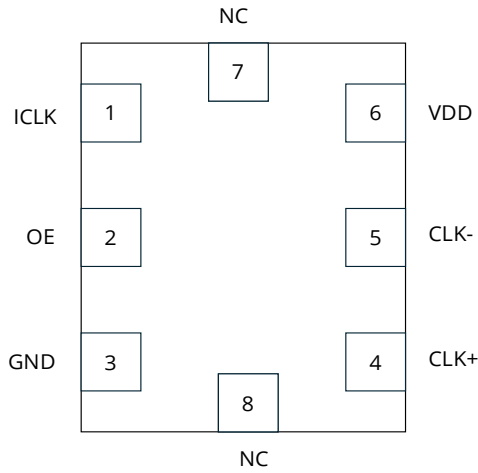


Figure 2. MS1510 Pin Assignments

Table 1. MS1510 Pin Descriptions

Pin No	Name	Description
1	ICLK	Reference CLK input
2	OE	Output Enable
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply
7	NC	No Connect
8	NC	No Connect

Specifications

Table 2. Electrical Specifications

Typical values are specified at $T_A = 25^\circ\text{C}$, $V_{DD} = 1.8\text{V}$ unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
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Frequency Range

Input Frequency Range	I_{CLK}		1		750	MHz
Input Voltage Swing	I_{SWG}	AC-coupled	0.1		1.8	V _{pp-SE}
Output Frequency Range	F_{CLK}	All Output Formats	20		2200	MHz

Clock Output Jitter Characteristics

RMS Phase Jitter (12 KHz – 20 MHz)	Φ_{JITTER}	Frequency= 491.52 MHz		21.6	32	fs
		Frequency= 625 MHz		19.6	30	fs

Note:

Phase jitter measured on Agilent 5052B Signal Source Analyzer

Operating Voltage/Temperature Range

Supply Voltage	V_{DD}		1.71	1.8	1.89	V
Temperature Range	T_A	Industrial Temperature	-40		85	$^\circ\text{C}$
		Extended Industrial Temperature	-40		105	$^\circ\text{C}$

Current Consumption

Supply Current	I_{DD}	LVDS Output (Output Enabled)	150	180	mA
		All Other Outputs (Output Enabled)	160	190	mA
		Tristate Hi-Z (Output Disabled)	70	84	mA

Input Characteristics

Digital Input Levels (OE)	V_{IH}		$0.7XV_{DD}$		V
	V_{IL}			$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time		3	us
	T_E	Output Enable Time		20	us
Input Signal Powerup Time	T_{PWR}	Time required from $0.9xV_{DD}$ until input signal	10		ms
Output Lock Time	T_{LOCK}	Time from input signal to a stable output	10		ms

PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (312.5MHz)		-114	dBc
Power Supply-Jitter Sensitivity	PSJS			0.1	fs/mv

Note:

(1) Measured with 50 mVpp ripple from 50 KHz to 1 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		65	100	ps
LVDS Output (AC Mode)	V_{pp}	Differential Pk-Pk	0.5	0.7	0.9	V
LVDS Extended Output (AC Mode)	V_{pp}	Differential Pk-Pk	0.8	1.2	1.6	V
CML Output (AC Mode)	V_{pp}	Differential Pk-Pk	0.6	0.8	1	V
LVPECL Output (AC Mode)	V_{pp}	Differential Pk-Pk	1.2	1.4	1.6	V
HCSL Output	V_{pp}	Differential Pk-Pk	1.1	1.35	1.6	V
HCSL Output Voltage	V_{CM}	Common Mode Voltage	340	350	360	mV

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C

Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.

Table 4. Environmental Compliance

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Moisture Sensitivity Level (MSL)	3

Note: For additional information not listed, please contact Mixed-Signal Devices.

Table 5. ESD Levels

Description	Description	Specification	Level
HBM ¹	Human Body Model	JEDEC JS-001	2000V
CDM ²	Charge Device Model	JEDEC JESD22-C101	500V

Notes:
 1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155
 2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157

Table 6. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
3.2mmX2.5mm 8 pin LGA	Thermal Resistance, Junction to Ambient	θ_{JA}	80	°C/W
	Thermal Resistance, Junction to Board	θ_{JB}	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C

Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.

Table 7. Typical Output Phase Noise Characteristics

VDD= 1.8V, T_A= 25°C, Output Type = LVDS-EXT

Offset frequency	312.5 MHz	491.52 MHz	625 MHz	1250 MHz	1600 MHz	Unit
1 KHz	-103	-98	-99	-93	-91	dBc/Hz
10 KHz	-132	-130	-127	-122	-119	dBc/Hz
100 KHz	-154	-152	-149	-143	-142	dBc/Hz
1 MHz	-164	-160	-159	-152	-152	dBc/Hz
10 MHz	-165	-161	-160	-151	-152	dBc/Hz
20 MHz	-166	-161	-160	-153	-152	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	21.8	21.6	19.6	21.7	18.8	fs

Typical Output Measured Phase Noise Plots

This section shows four MS1510 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent 5052B Signal Source Analyzer.

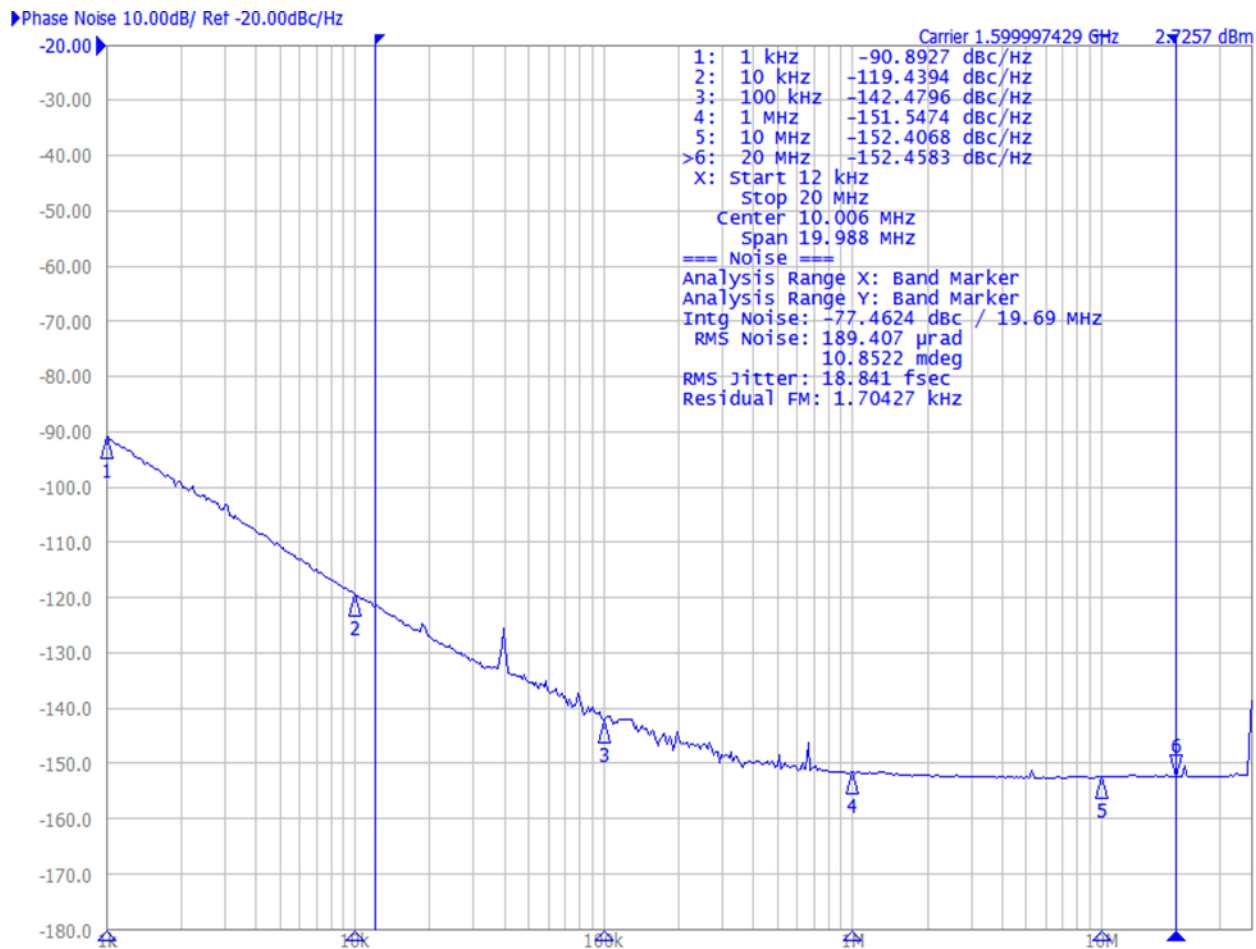


Figure 3. Carrier: 1600 MHz

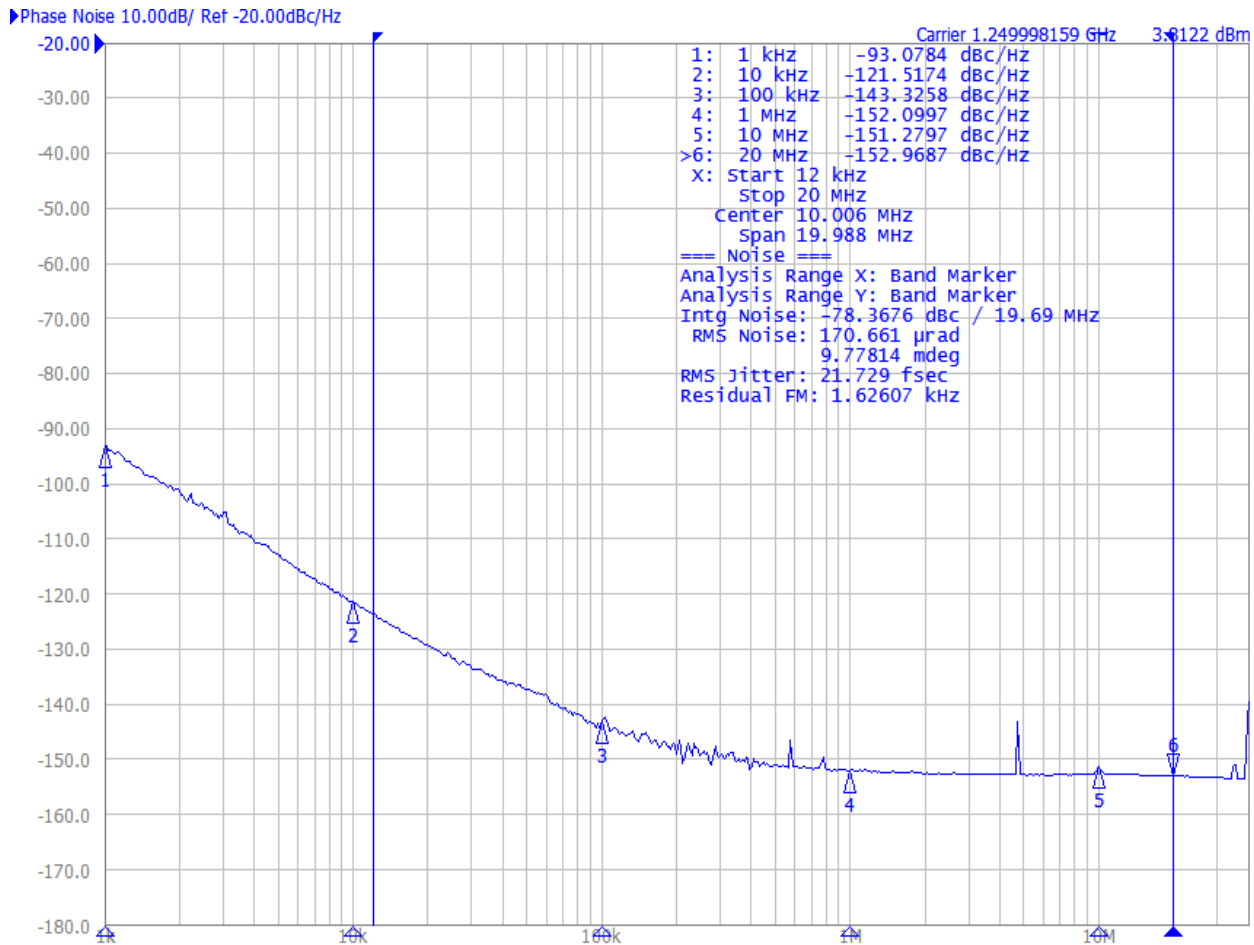


Figure 4. Carrier: 1250 MHz

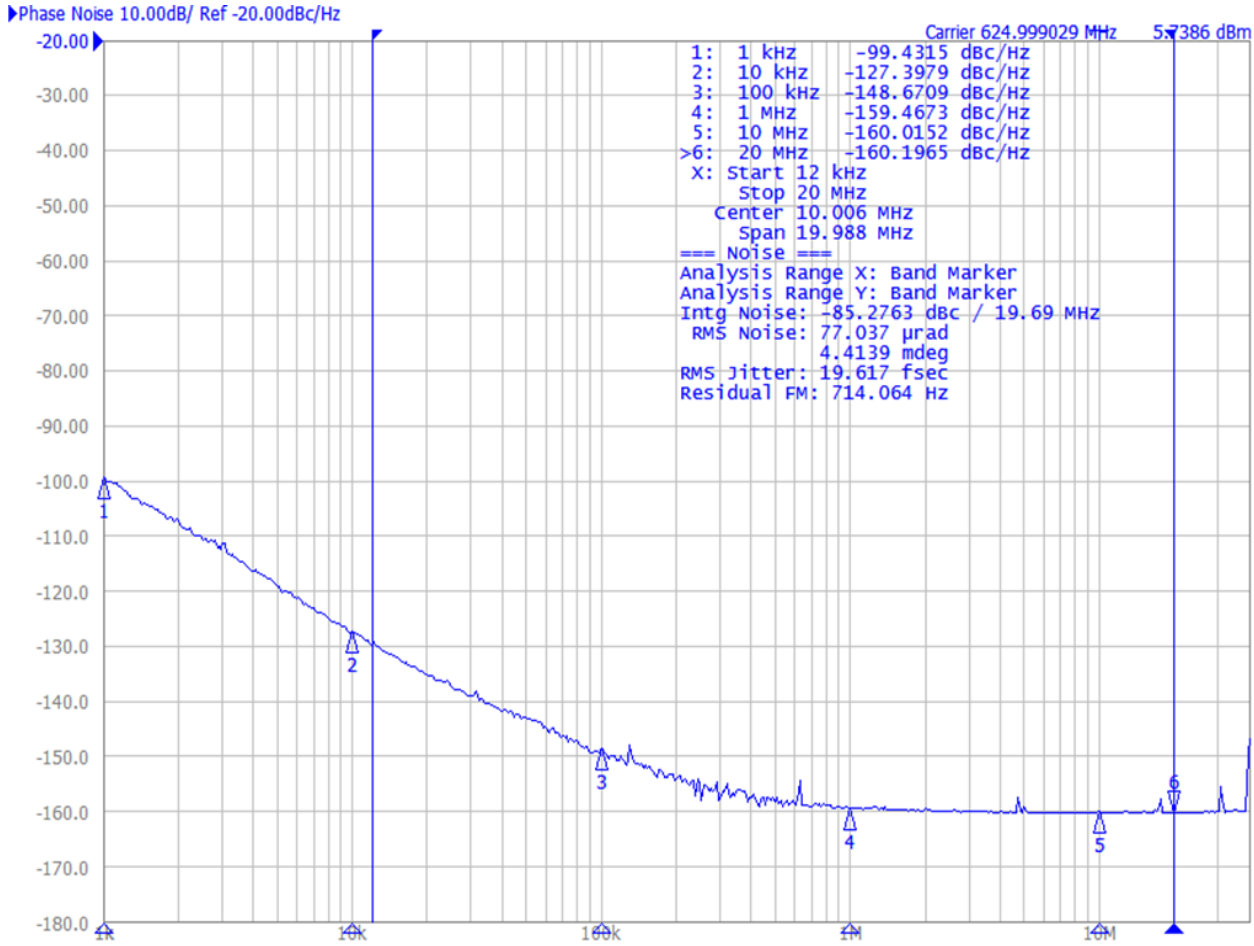


Figure 5. Carrier: 625 MHz

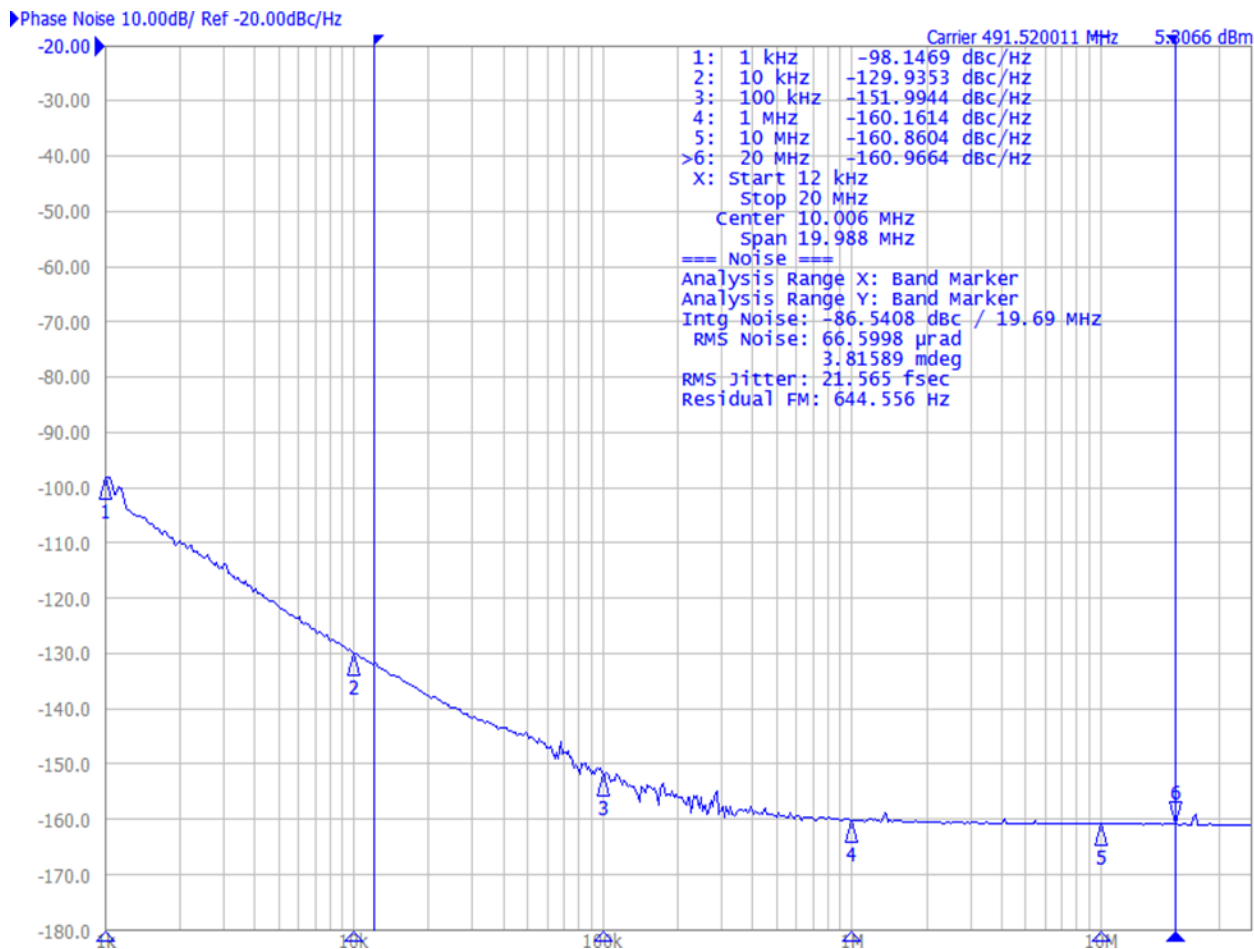


Figure 6. Carrier: 491.52 MHz

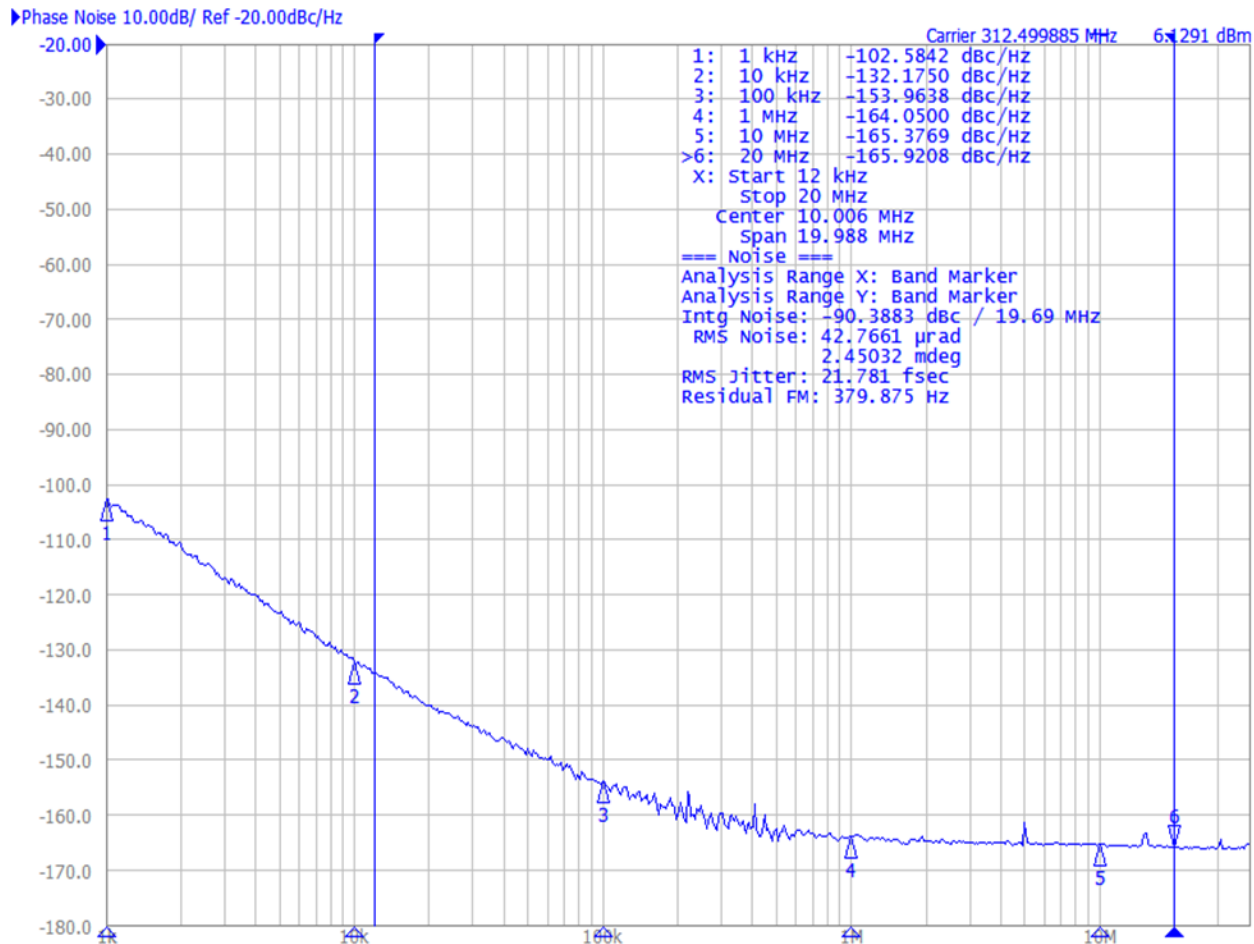


Figure 7. Carrier: 312.5 MHz

Overview

The MS1510 is a single channel high-performance Jitter Attenuator that offers exceptional capabilities in the generation of an ultra-low phase noise clock, making it an ideal solution for next-generation communication systems and base stations. This device can produce one differential output clock synchronized to the reference clock input with input frequency ranging from 1MHz to 750MHz single-ended, and gapped clock support. The MS1510 boasts an output frequency range of 20MHz to 2.2GHz and a remarkably low RMS jitter of 20fs (12KHz to 20MHz), making it one of the most reliable and precise devices available.

The device's programmability is configured by on-chip non-volatile memory (NVM). This attribute permits the MS1510 to provide great flexibility and ease of use in a broad range of applications, including telecommunications, networking, and test and measurement equipment.

Functional Description

MS1510 is an all-digital clock generation device that incorporates a range of features to enable jitter attenuation and programmable multiplication of input frequency. It receives one reference clock input and generates any multiplication of the input clock using fractional multipliers and high-speed output divider. The device can output various formats, such as LVDS, LVDS EXT, CML, LVPECL, and HCSL.

1. Frequency Configuration

The frequency configuration is defined through non-volatile memory (NVM). Device settings are programmed during manufacturing and are automatically loaded at power-up. A combination of fractional frequency synthesis (M/N) and integer output division (R_n) allows generation of a wide range of output frequencies across all outputs. Frequency planning parameters are calculated using the EZ-Cleaner™ GUI utility, which generates the required configuration values for NVM programming. Contact Mixed-Signal for the EZ-Cleaner™ GUI utility.

2. Jitter Attenuation Bandwidth Control

The MS1510 provides digitally programmable jitter attenuation bandwidth control, which defines the degree of input reference jitter filtering. Bandwidth options from 0.01 Hz to 4 kHz are selectable during configuration and stored in NVM.

Because jitter filtering and frequency synthesis are implemented entirely in the digital domain, the device maintains inherent stability across all supported bandwidth settings, with less than 0.1 dB of peaking, independent of the selected bandwidth.

Operation Modes

Free Running Mode (Default Mode)

After initialization, MS1510 will enter free running mode. In this mode, the device generates an output clock using multiplication factor stored in the on-chip NVM. The frequency accuracy of the generated output clock tracks the frequency accuracy of the input reference. For example, if the input frequency is 156.25 MHz (+/- 10ppm) and the stored multiplication factor is 33/32, the output frequency would be 161.1328125 MHz (+/- 10ppm).

Frequency Translation Example

For example, if the input frequency is 15.625 MHz (± 10 ppm) and the stored multiplication factor is 33/32, the resulting output frequency is:

$$F_{\text{OUT}} = F_{\text{IN}} \times (M/N)$$
$$F_{\text{out}} = 156.25 \text{ MHz} \times (33/32) = 161.1328125 \text{ MHz}$$

The output frequency tolerance directly tracks the input reference tolerance:

$$\Delta F_{\text{OUT}} = \Delta F_{\text{IN}}$$

Lock Acquisition Mode.

Upon completion of the configuration process, the MS1510 will transition into the lock acquisition mode. This mode comprises two stages: fast acquisition and narrow acquisition. In the first stage, the loop bandwidth is widened to facilitate a speedy initial acquisition process. Following this, the bandwidth is narrowed as the device completes the lock.

Output

MS1510 supports CML, LVDS, LVDS-EXT, LVPECL, and HCSL output formats. The output enable, OE, is active HI. When OE is LOW, MS1510 output will be High Z but the loop will stay locked.

Input Terminations

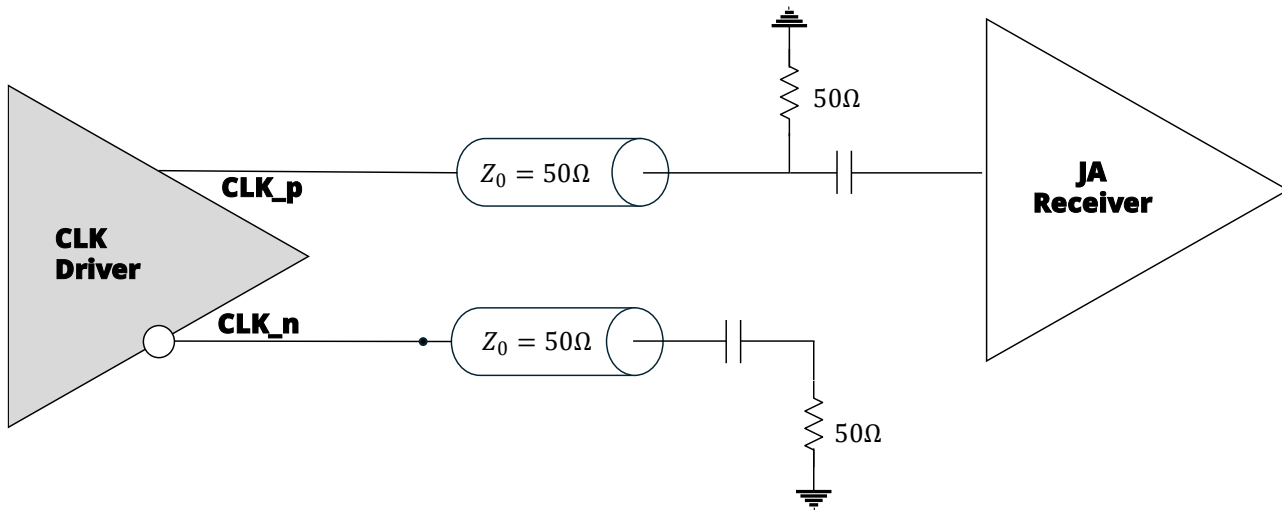


Figure 8. Differential Input Interface

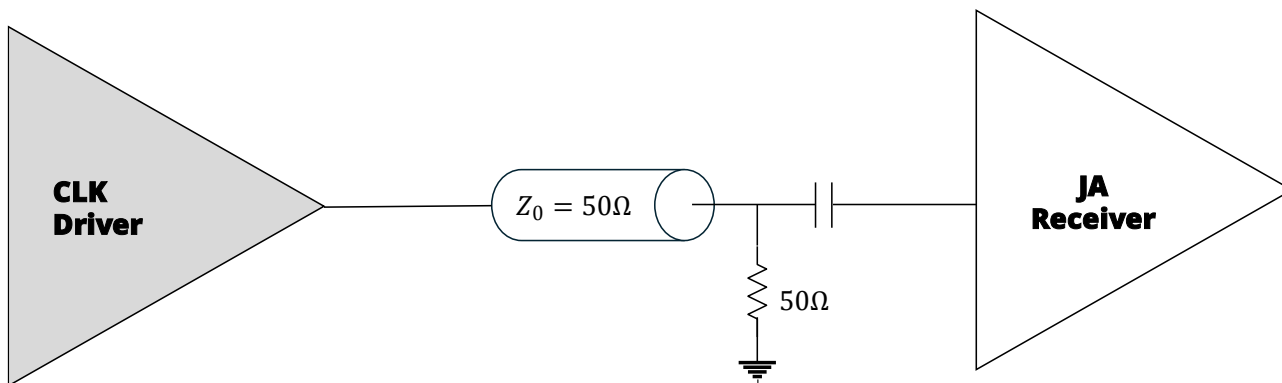


Figure 9. Single-Ended Input Interface

Output Terminations

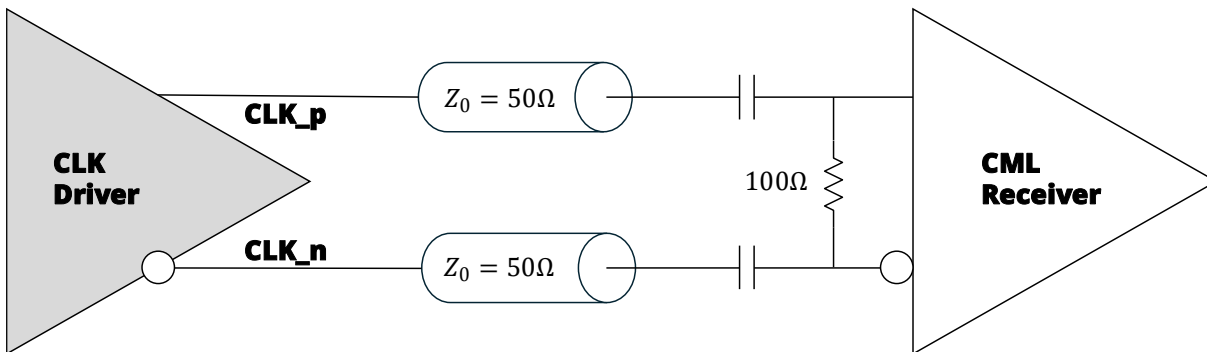


Figure 10. AC-Coupled CML

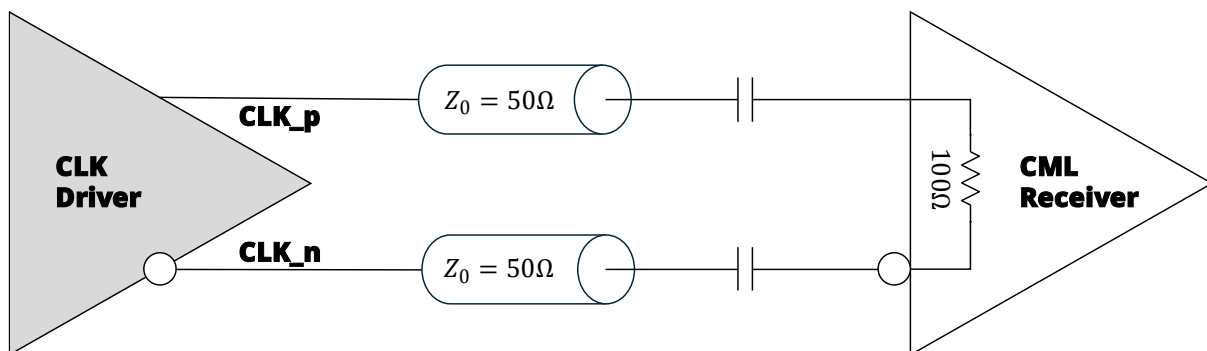


Figure 11. AC-Coupled CML (Receiver Termination)

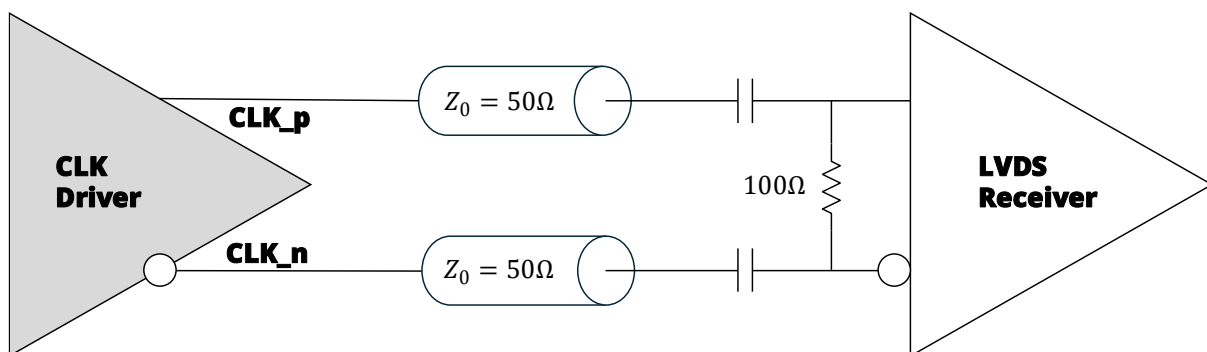


Figure 12. AC-Coupled LVDS

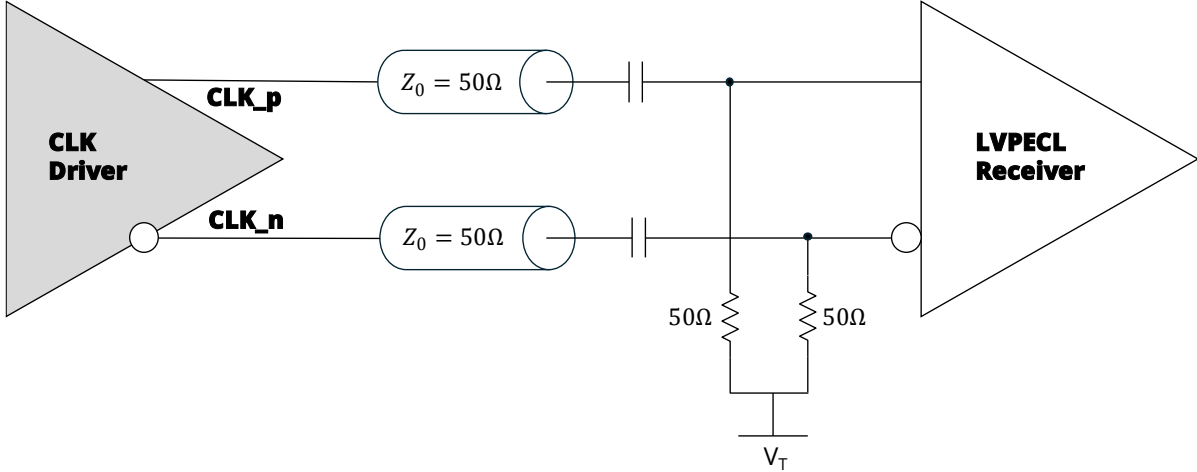


Figure 13. AC-Coupled LVPECL

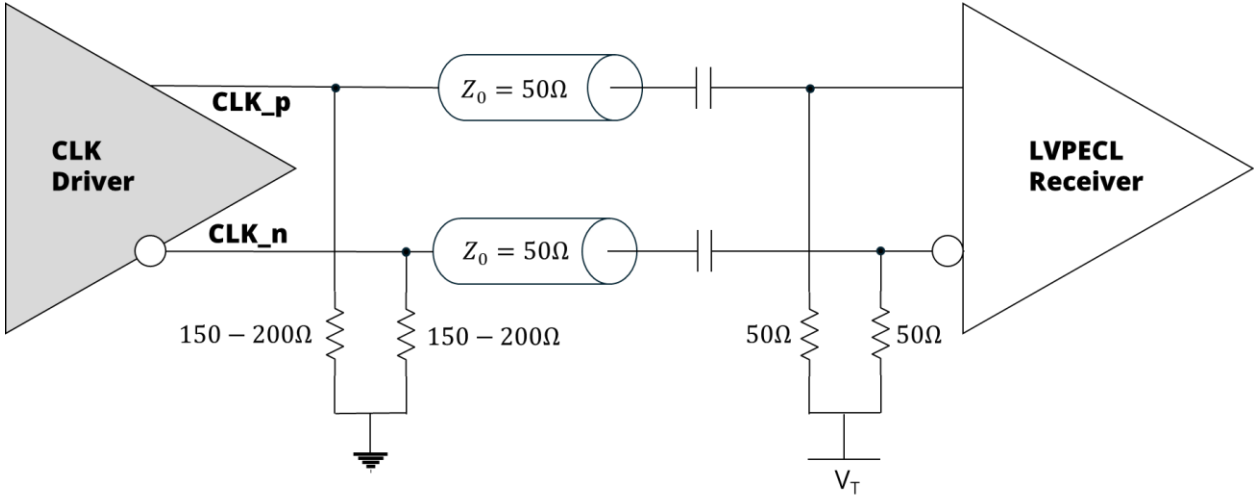


Figure 14. AC-Coupled LVPECL (DC Bias Resistor)

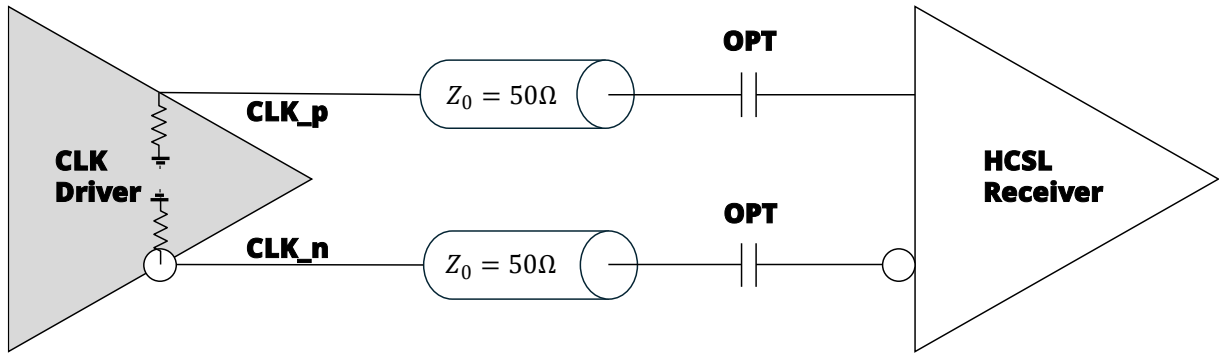


Figure 15. HCSL (Integrated Termination)

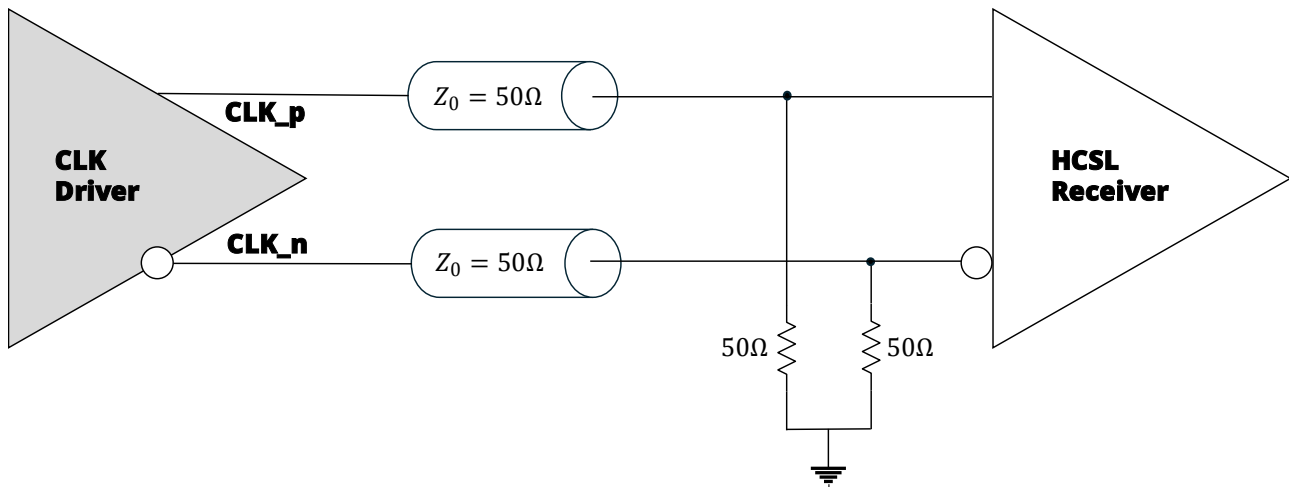


Figure 16. DC-Coupled HCSL (Receiver Termination)

Output Timing

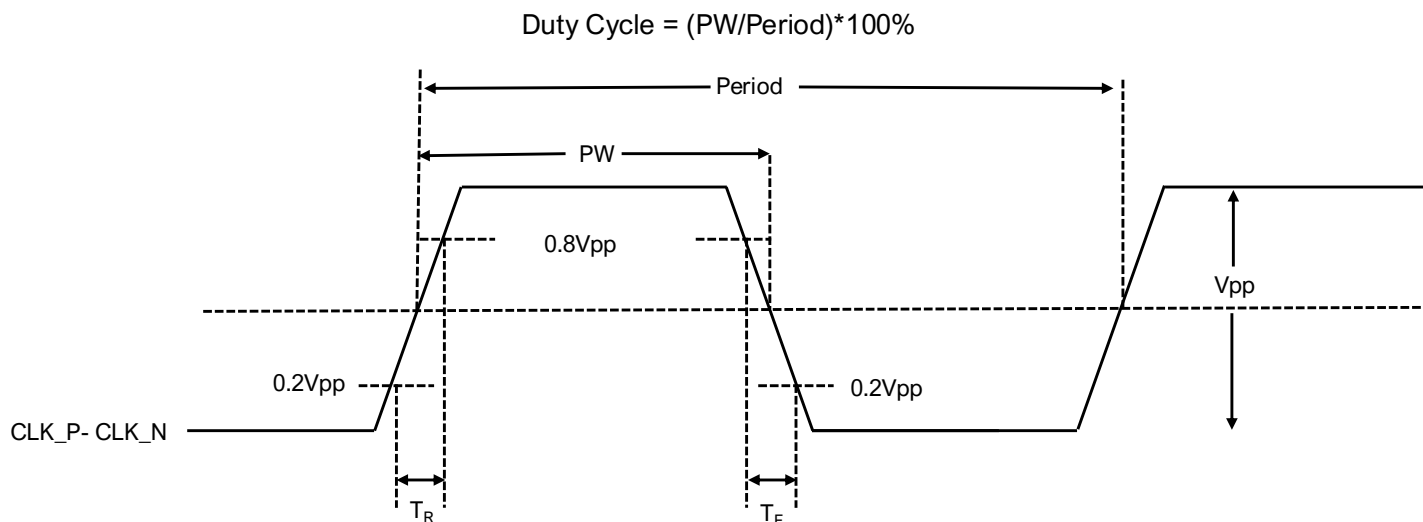


Figure 17. Output Timing across differential pair (CLK_P-CLK_N)

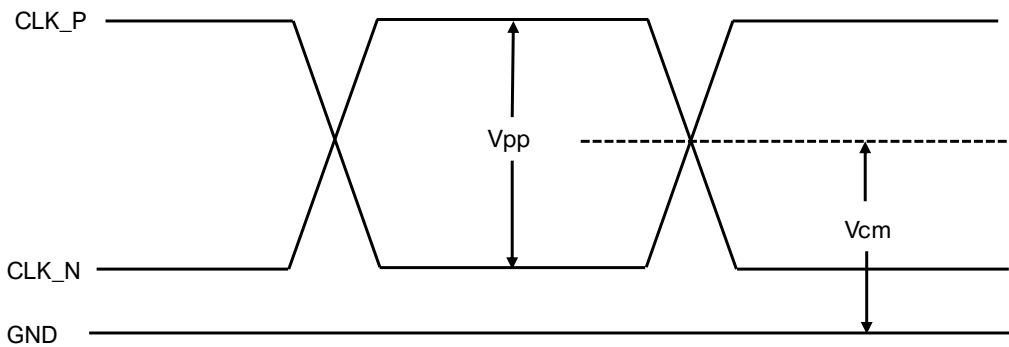


Figure 18. HCSL Output Level across differential pair (CLK_P-CLK_N)

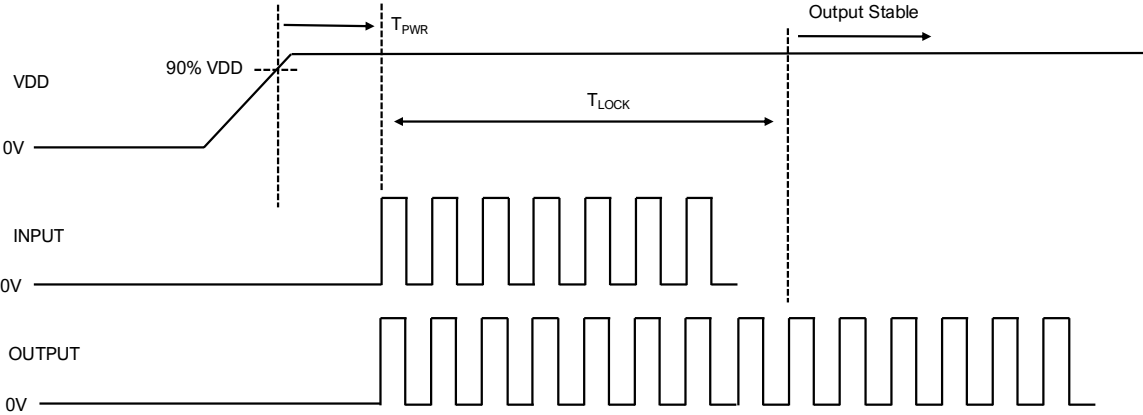


Figure 19. Powerup Timing Input/Output

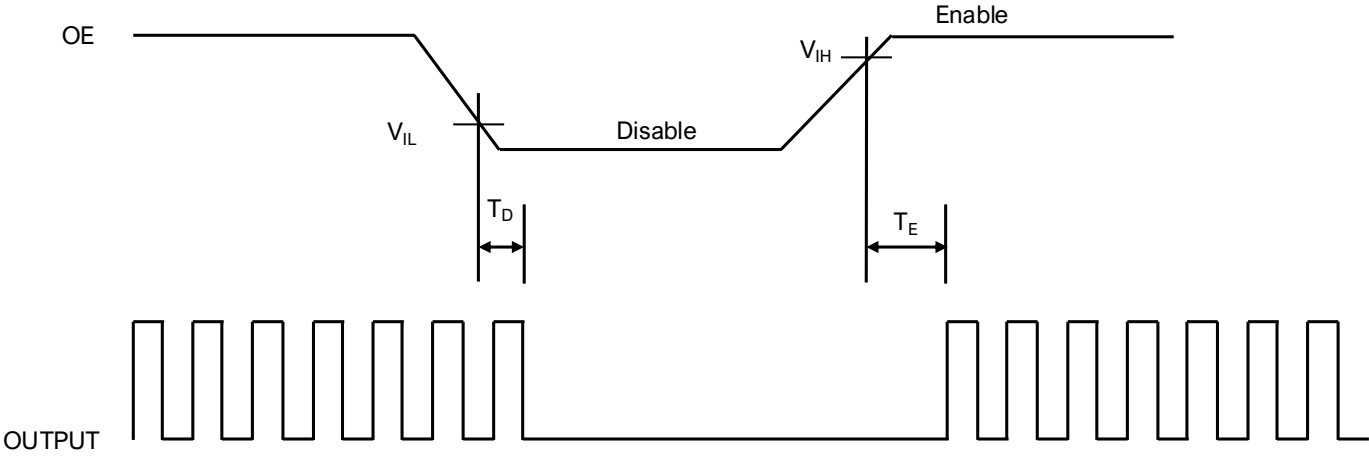


Figure 20. OE Enable/Disable Timing

Packaging Information

Figure 21 shows the MS1510 packaging drawing.

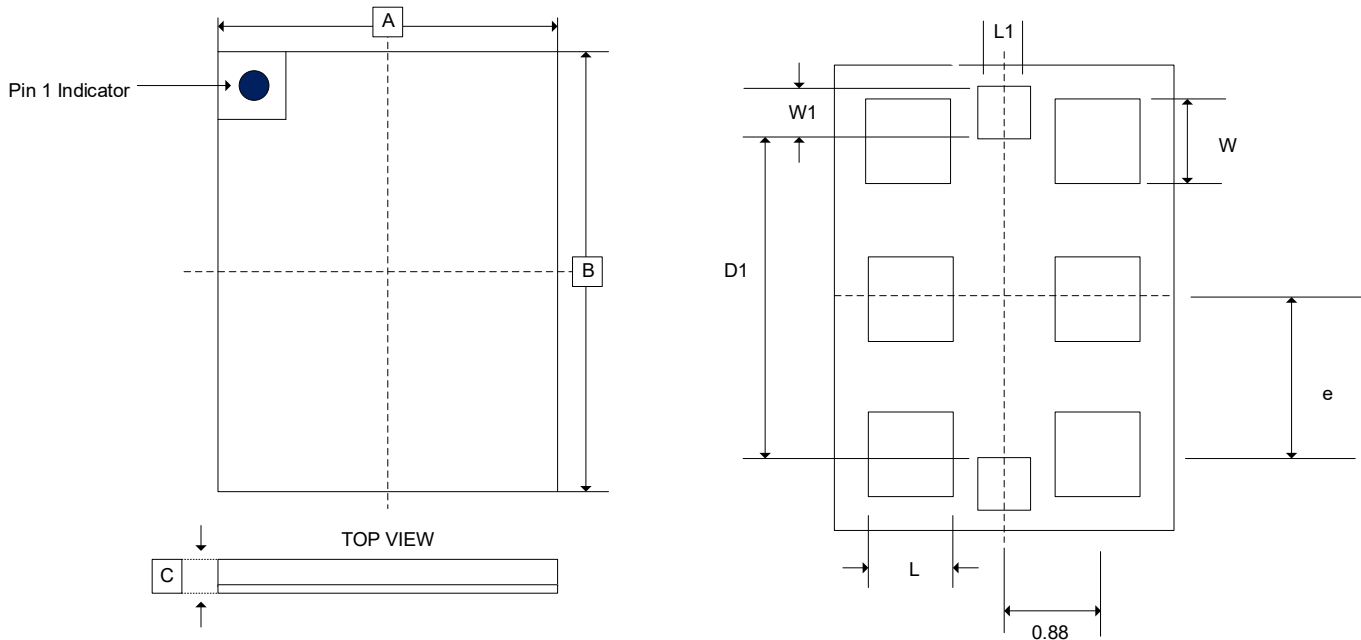


Figure 21. MS1510 Packaging Drawing (3.2mm x 2.5 mm)

Table 8. MS1510 Packaging Dimensions

Dimensions	Min	Nom	Max
A	2.5 BSC		
B	3.2 BSC		
C	1.246	1.346	1.446
W	0.55	0.6	0.65
L	0.5	0.55	0.6
W1	0.35	0.4	0.45
L1	0.35	0.4	0.45
e	1.1 BSC		
D1	2.2 BSC		
Package Edge Tolerance	0.1		
Mold Flatness	0.1		
Coplanarity	0.08		

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 22 shows the MS1510 PCB land pattern.

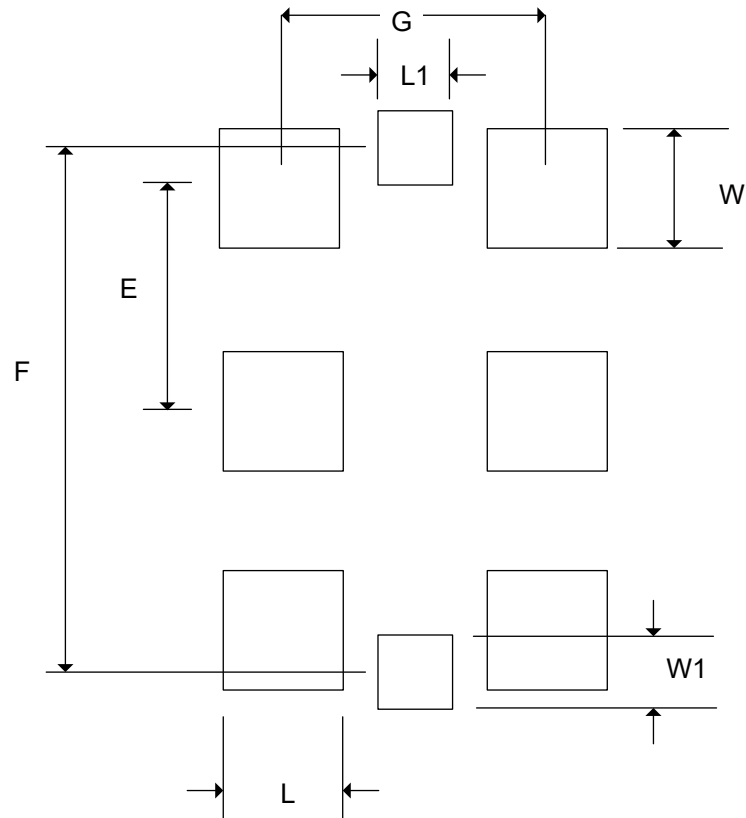


Figure 22. MS1510 Packaging Land Pattern Drawing (3.2mm x 2.5mm)

Table 9. MS1510 Packaging Land Pattern Dimensions

Dimensions	In mm
L	0.7
W	0.7
L1	0.5
W1	0.55
E	1.1
F	2.6
G	1.76

Device Top Marking

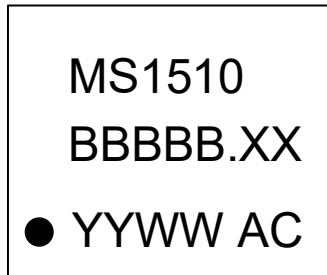


Figure 23. MS1510 Device Top Marking Showing Pin 1

Table 10. MS1510 Device Marking Legend

Line	Position	Description
1	1	Part Number
2	1-5	Wafer Lot Number
	6-7	Wafer #
3	Lot Traceability	
	1	Pin 1 Orientation Mark (Dot),
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	6-7	Assembly Code

Part Ordering Information

Figure 24 shows a logic tree for ordering each of the three available parts.

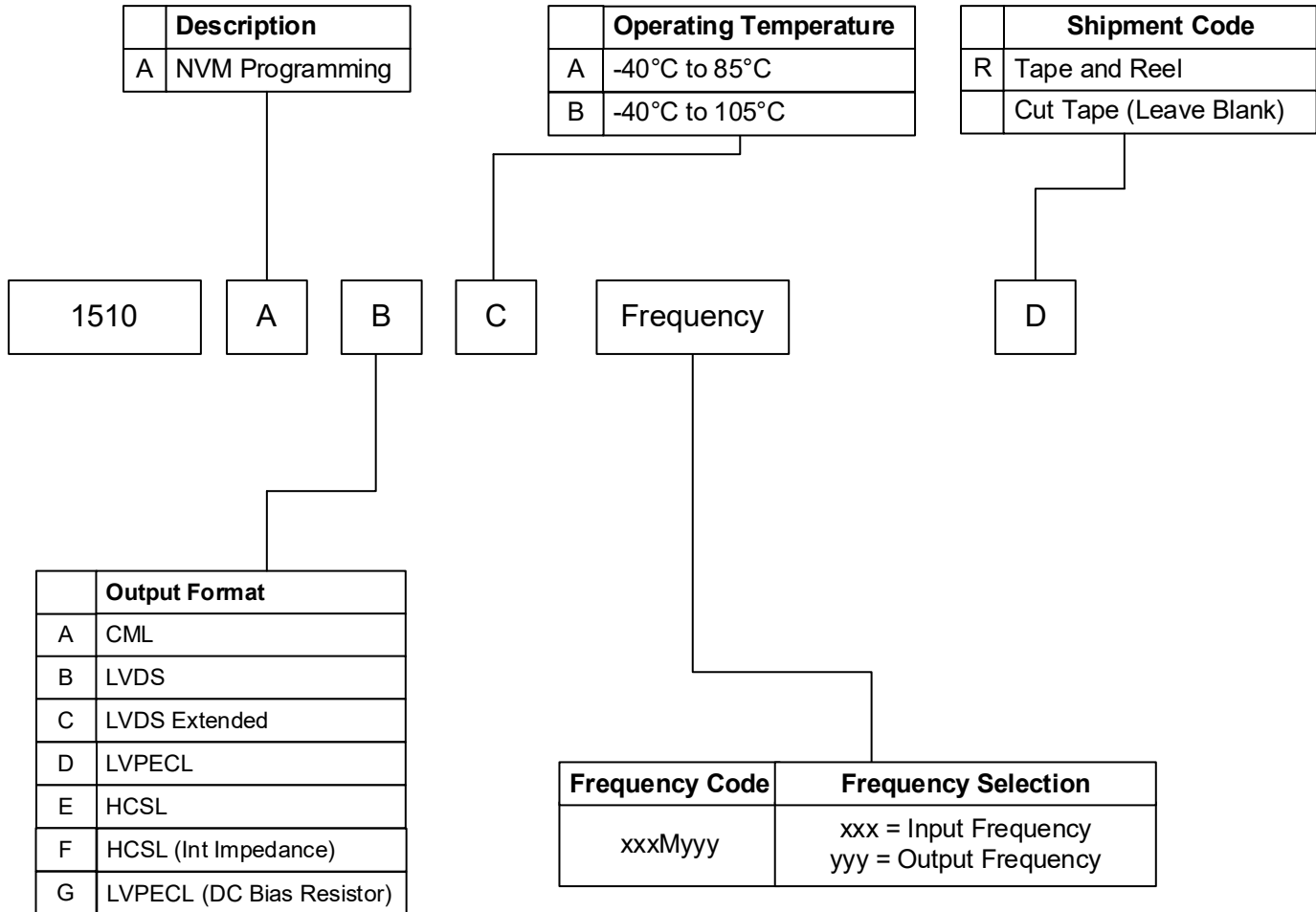


Figure 24. MS1510 Part Ordering Information

Table 11. Example of ordering part number

Base P/N	Output Format	Operating Temperature	Input Frequency	Output Frequency	Shipment Type	Ordering part number
1510	HCSL	-40°C to 85°C	156 MHz	312.5 MHz	Tape and Reel	1510AFA156M312R
1510	LVPECL	-40°C to 105°C	312.5 MHz	1250 MHz	Tape and Reel	1510ADB312MC50R

Input/Output Frequency codes for ordering

Code (xxx)	Frequency (MHz)	Code (yyy)	Frequency (MHz)
001	1	100	100
100	100	106	106.25
106	106.25	122	122.88
122	122.88	153	153.6
153	153.6	156	156.25
156	156.25	212	212.5
212	212.5	245	245.76
245	245.76	250	250
250	250	307	307.2
307	307.2	312	312.5
312	312.5	322	322.2656525
322	322.2656525	491	491.52
491	491.52	500	500
500	500	614	614.4
614	614.4	625	625
625	625	644	644.53125
644	644.53125	983	983.05
750	750	C50	1250

Please contact Mixed-Signal Devices for additional frequency codes

Reflow Profile (IPC/JEDEC-STD-020)

Figure 25 shows the reflow profile for MS1510

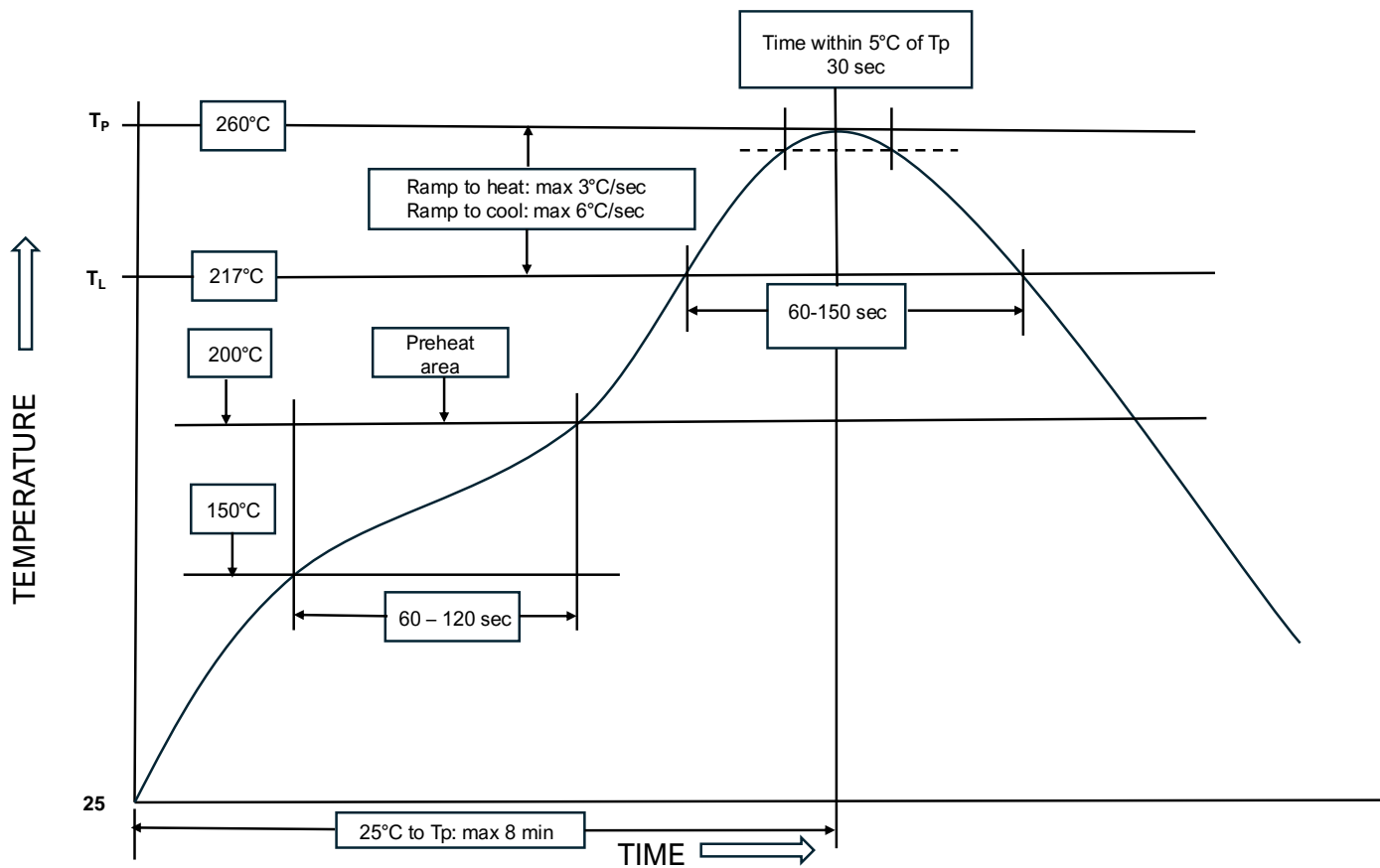


Figure 25. MS1510 Reflow Profile

REVISION HISTORY

Revision 1.5

April 20, 2026

- Added LVPECL Load Termination
- Updated ordering part number (include LVPECL Load Termination)

Revision 1.4

January 5, 2026

- Updated Overview section

Revision 1.3

November 14, 2025

- Updated Product Title

Revision 1.2

October 17, 2025

- Updated Figure 13: Output Driver (HCSL); removed AC coupling
- Updated ordering part number

Revision 1.1

September 2, 2025

- Added Timing Diagram
- Updated Output Driver information (LVPECL, HCSL)
- Added Reflow Profile

Revision 1.0

December 20, 2024

- Initial Release

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