

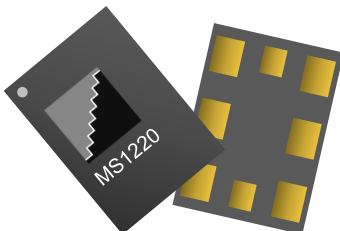
## Ultra-Low Jitter Voltage Controlled Crystal Oscillators (VCXO)

### Features

- Available at any frequency from 10 MHz to 1000 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 34.9 fs at 156.25 MHz
  - 24.6 fs at 312.50 MHz
  - 26.1 fs at 491.52 MHz
  - 26.8 fs at 625 MHz
- Total stability of  $\pm 1$  ppm
- Programmable tuning slope (Kvco) up to 300 ppm/V
- CML/LVDS/LVDS-EXT/LVPECL/HCSL output formats
- Simplified BoM with no external loop filters
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Industry standard 3.2X2.5 mm 8-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

### Applications

- SONET/SDH
- 10 GbE LAN/WAN
- Wireless Infrastructure
- Synchronous Ethernet
- Optical modules
- Clock and data recovery
- Clock Generation and Frequency Translation
- High-performance replacement for SAW



### General Description

The MS1220 is a voltage-controlled crystal oscillator (VCXO) powered by our Virtual Crystal™ technology that enables ultra stable fully programmable multi-GHz clocks with extremely low phase noise.

Adaptive fully autonomous DSP algorithms running in the background continuously monitor and ensure robust and consistent performance over process, voltage, and temperature variations.

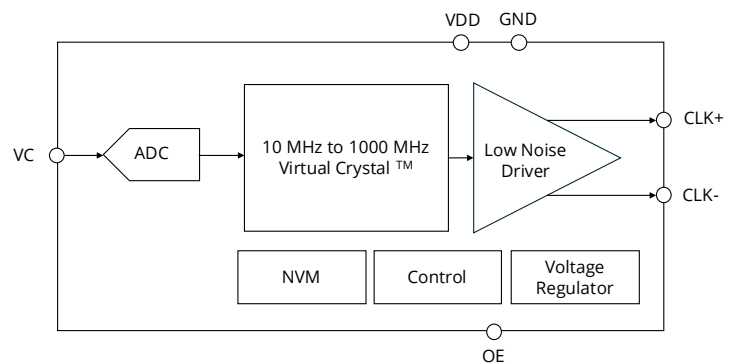
The devices are factory programmed to provide any frequency between 10 MHz and 1000 MHz with less than 1 ppb resolution.

The MS1220 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

### Device Information

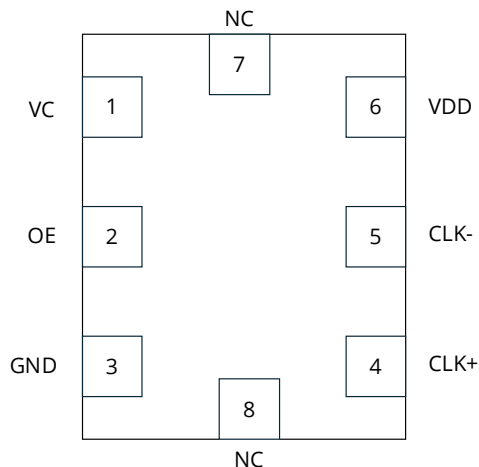
Part Number	Package	Description
MS1220	3.2X2.5 mm 8-pin LGA	VCXO

Figure 1. Functional Block Diagram



**MS1220**

**Pin Assignment and Pin Description**



**Figure 2. MS1220 Pin Assignments**

**Table 1. MS1220 Pin Descriptions**

Pin No	Name	Description
1	VC	Control Voltage
2	OE	Output Enable
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply
7	NC	No Connect
8	NC	No Connect

## Specifications

**Table 2. Electrical Specifications**

Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V}$  unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination. A 0.1 $\mu\text{F}$  and 10 $\mu\text{F}$  bypass capacitor should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
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### Frequency Range

Frequency Range	$F_{\text{CLK}}$	All Output Formats	10		1000	MHz
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### Frequency Stability

Frequency Stability (Temperature)	$F_{\text{TS}}$	$-40^\circ\text{C}$ to $105^\circ\text{C}$	-1		1	ppm
Frequency Tolerance	$F_{\text{INIT}}$	$25^\circ\text{C} \pm 2^\circ\text{C}$ , after 2x flow soldering	-1		+1	ppm
First Year Aging	$F_{\text{1yr}}$	$25^\circ\text{C} \pm 2^\circ\text{C}$	-1		1	ppm

### Clock Output Jitter Characteristics

RMS Phase Jitter (12 KHz – 20 MHz)	$\Phi_{\text{JITTER}}$	Frequency=312.5 MHz		24.6	37	fs
		Frequency=625 MHz		26.8	40	fs

**Note:**

Phase jitter measured on Agilent 5052B Signal Source Analyzer

### Operating Voltage/Temperature Range

Supply Voltage	$V_{\text{DD}}$		1.71	1.8	1.89	V
Temperature Range	$T_A$	Industrial Temperature	-40		85	$^\circ\text{C}$
		Extended Industrial Temperature	-40		105	$^\circ\text{C}$

**Current Consumption**

Supply Current	$I_{DD}$	LVDS Output (Output Enabled)	80	100	mA
		All Other Outputs (Output Enabled)	90	110	mA
		Tristate Hi-Z (Output Disabled)	50	60	mA

**Input Characteristics**

Digital Input Levels (OE)	$V_{IH}$		$0.7XV_{DD}$		V
	$V_{IL}$			$0.3XV_{DD}$	V
Output Enable (OE)	$T_D$	Output Disable Time		3	Us
	$T_E$	Output Enable Time		20	Us
Powerup Time	$T_{PWR}$	Time from $0.9xV_{DD}$ until output frequency ( $F_{CLK}$ ) within spec		10	Ms

**PSRR Characteristics**

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (312.5MHz)		-114	dBc
Power Supply-Jitter Sensitivity	PSJS			0.1	fs/mv

**Note:**

(1) Measured with 50 mVpp ripple from 50 KHz to 1 MHz applied on VDD Pin

## Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% $V_{PP}$ )	$T_R / T_F$	All Output Formats		65	100	ps
LVDS Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	0.5	0.7	0.9	V
LVDS Extended Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	0.8	1.2	1.6	V
CML Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	0.6	0.8	1	V
LVPECL Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	1.2	1.4	1.6	V
HCSL Output	$V_{pp}$	Differential Pk-Pk	1.1	1.35	1.6	V
HCSL Output Voltage	$V_{CM}$	Common Mode Voltage	340	350	360	mV

## Vc Control Voltage Input

Parameter	Symbol	Test Condition/Comment	Min		Typ	Max	Unit
Control Voltage Tuning Slope <sup>1</sup>	Kvco	0.1V to 0.9V			50		ppm/V
					100		
					150		
					200		
					250		
					300		
Control Voltage Linearity	Lvc	Best Straight Line Fit	-1.5		±0.5	+1.5	%
		KVCO Variation	-10		±5	+10	%
Modulation Bandwidth	BW				10		kHz
Vc Input Impedance	Zvc		500				kΩ
Nominal Control Voltage	Vcnom	@fo			0.5		V
Control Voltage Tuning Range	Vc		0.1			0.9	V

**Table 3. Absolute Maximum Ratings**

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C
<b>Note:</b> Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

**Table 4. Package Thermal Information**

Package	Parameter	Symbol	Value	Unit
3.2mmX2.5mm 8 pin LGA	Thermal Resistance, Junction to Ambient	θ <sub>JA</sub>	80	°C/W
	Thermal Resistance, Junction to Board	θ <sub>JB</sub>	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T <sub>J</sub>	125	°C
<b>Note:</b> The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

**Table 5. Environmental Compliance**

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Moisture Sensitivity Level (MSL)	3
Note: For additional information not listed, please contact Mixed-Signal Devices.	

**Table 6. ESD Levels**

Description	Description	Specification	Level
HBM <sup>1</sup>	Human Body Model	JEDEC JS-001	2000V
CDM <sup>2</sup>	Charge Device Model	JEDEC JESD22-C101	500V
<b>Notes:</b> 1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155 2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157			

**Table 7. Typical Output Phase Noise Characteristics**  
 VDD= 1.8V, T<sub>A</sub>= 25°C, Output Type = LVDS-EXT

Offset frequency	156.25 MHz	312.50 MHz	491.52 MHz	625 MHz	Unit
1 KHz	-106	-103	-100	-98	dBc/Hz
10 KHz	-138	-133	-128	-127	dBc/Hz
100 KHz	-157	-154	-149	-147	dBc/Hz
1 MHz	-167	-163	-158	-156	dBc/Hz
10 MHz	-168	-164	-160	-148	dBc/Hz
20 MHz	-168	-164	-159	-158	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	34.9	24.6	26.1	26.8	fs

### Typical Output Measured Phase Noise Plots

This section shows three MS1220 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent 5052B Signal Source Analyzer.

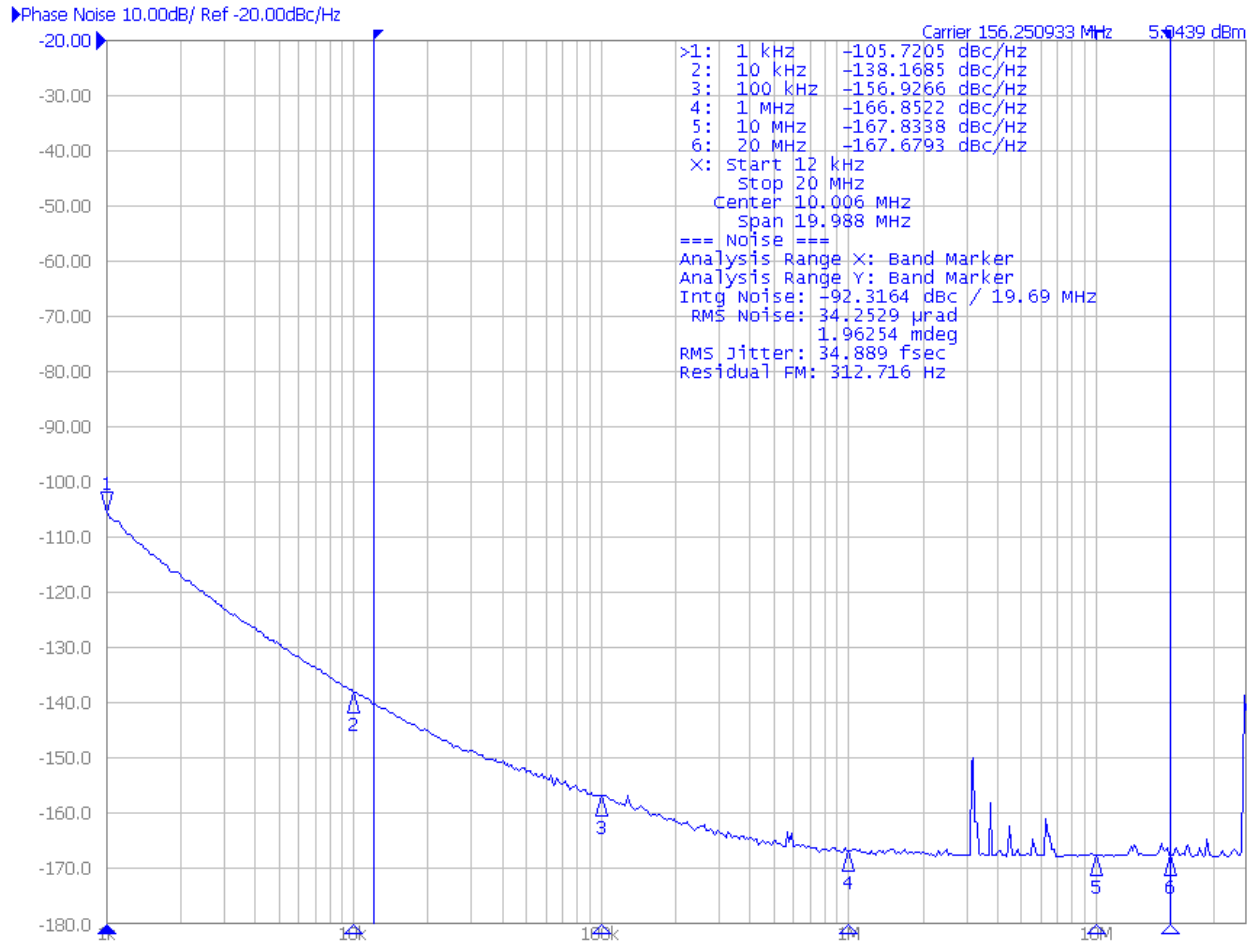


Figure 3. Carrier: 156.25 MHz

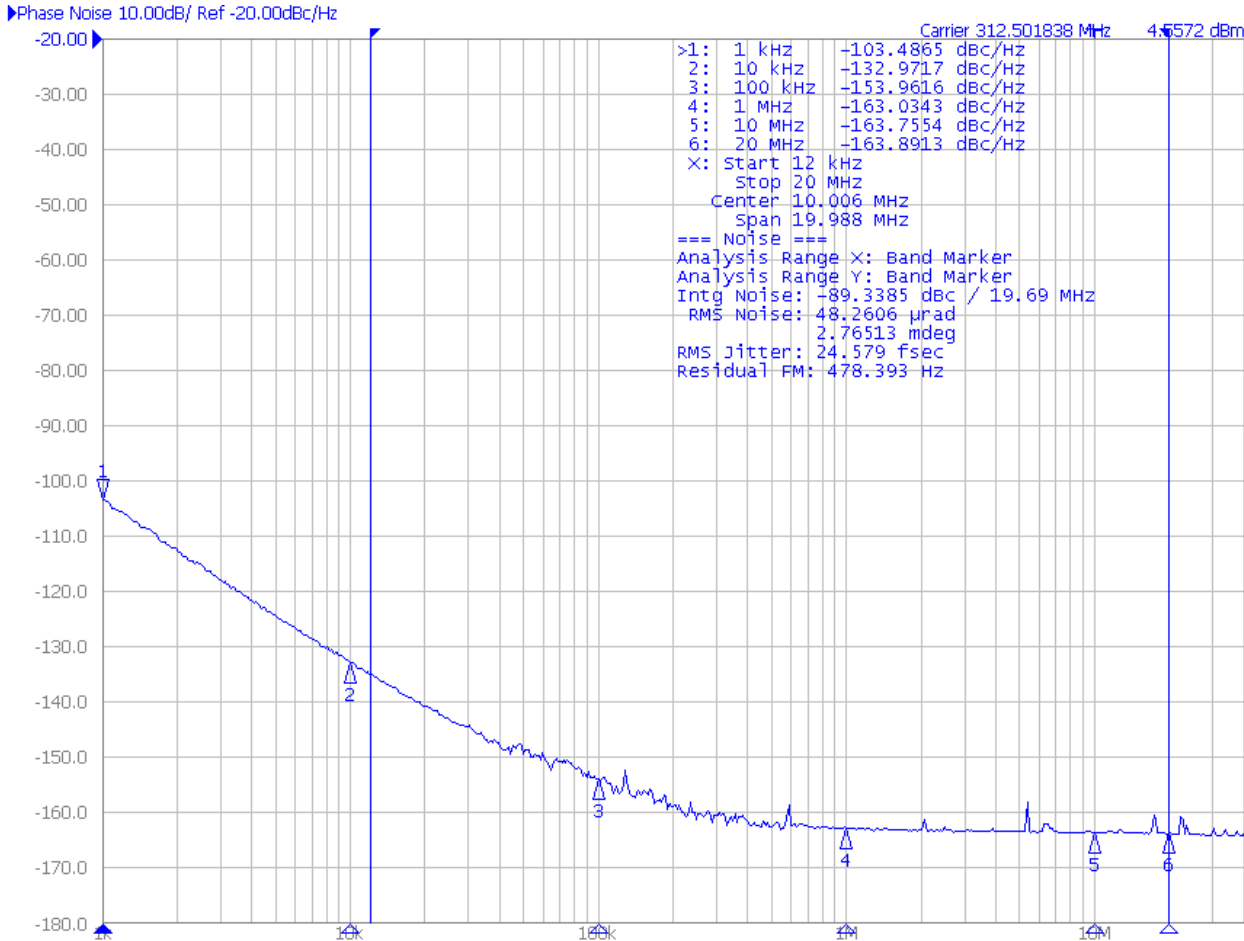


Figure 4. Carrier: 312.5 MHz

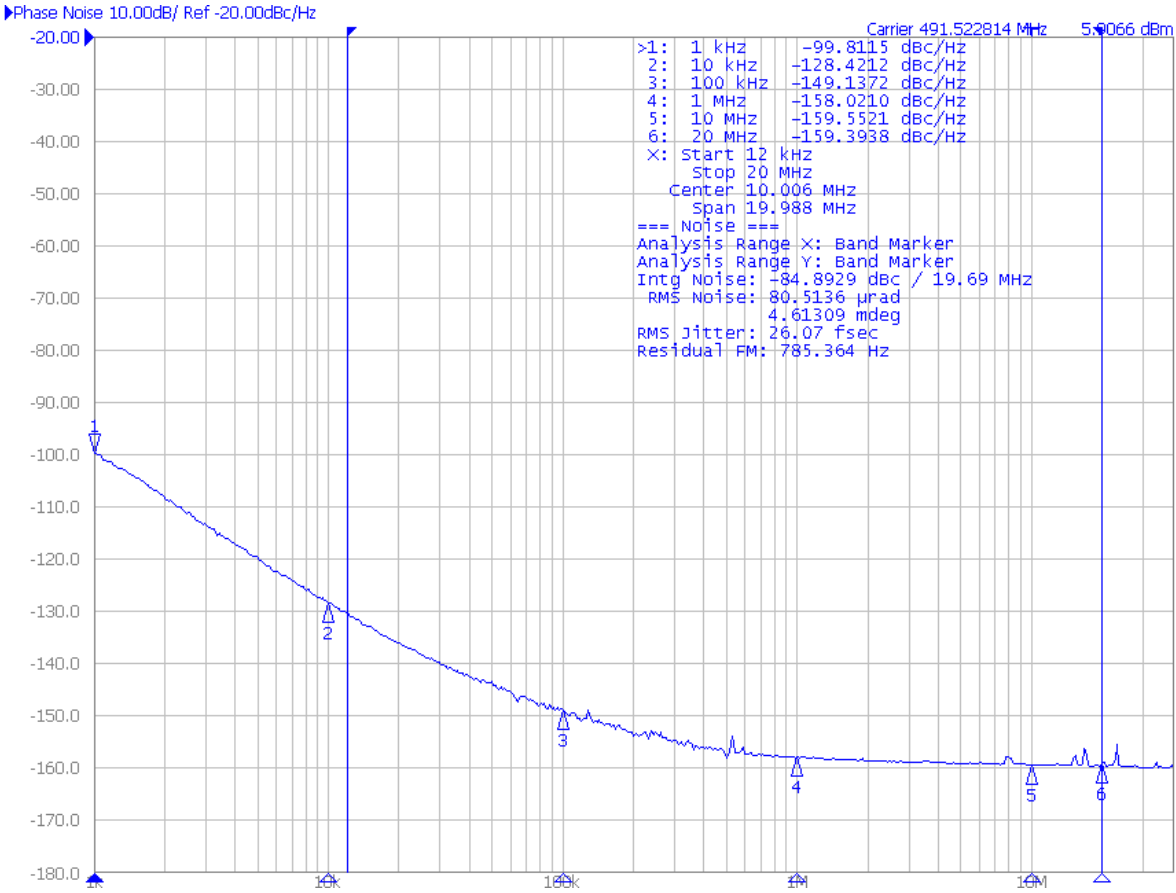


Figure 5. Carrier: 491.52 MHz

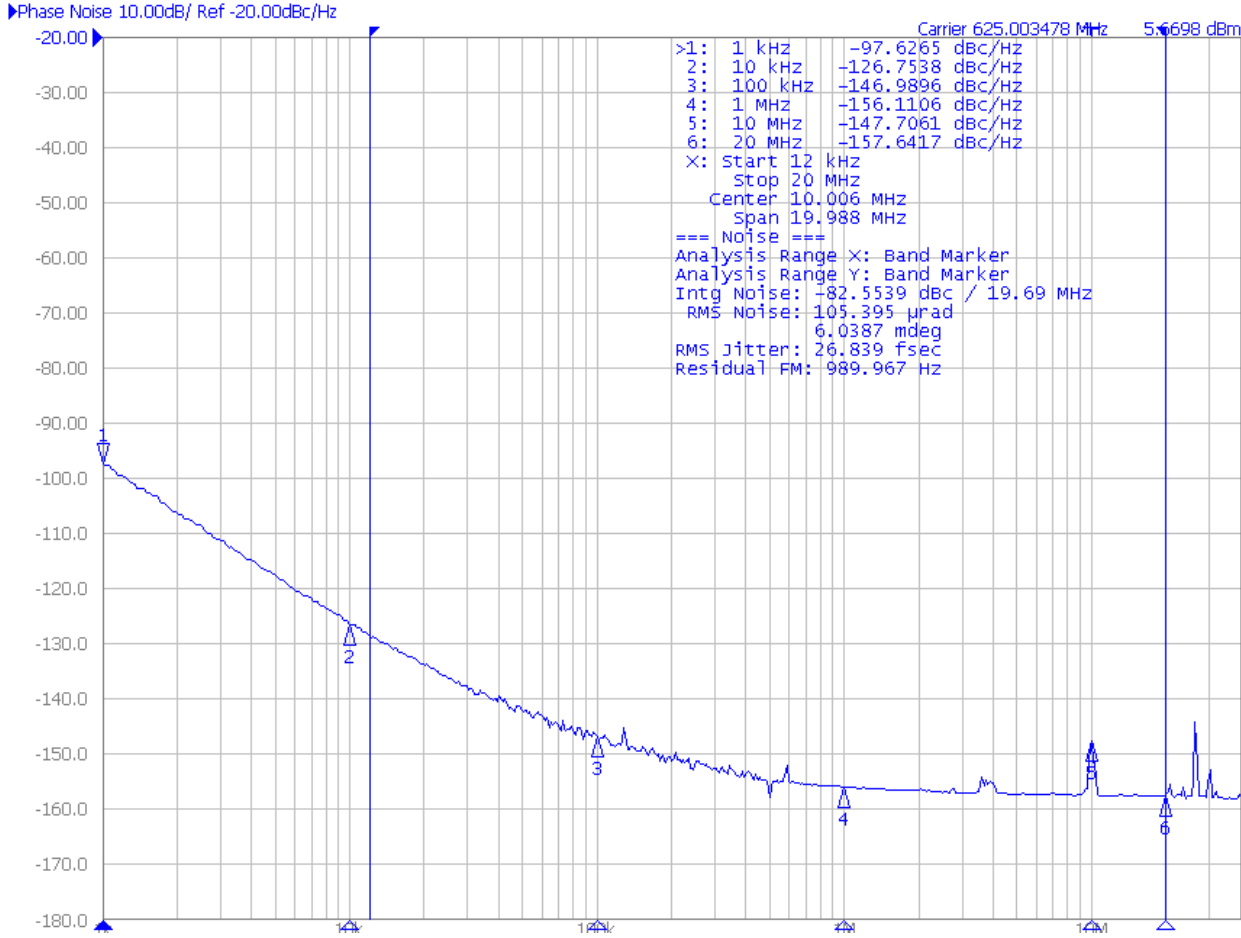


Figure 6. Carrier: 625 MHz

## Output Terminations

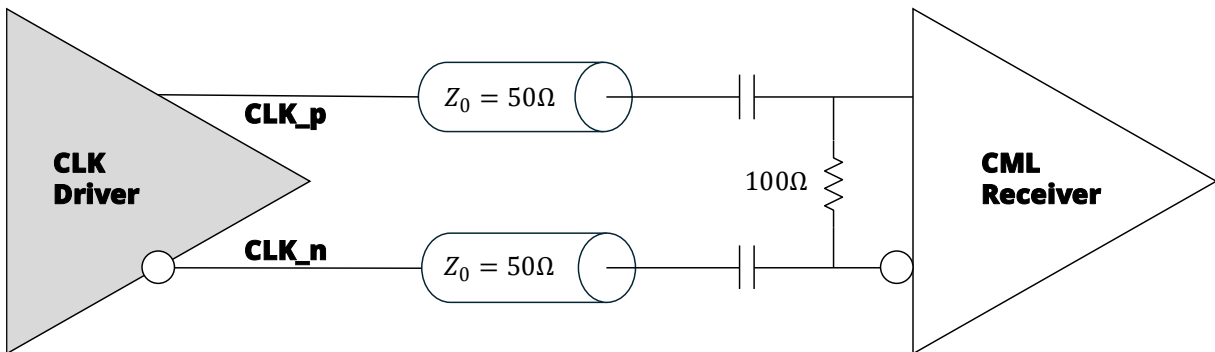


Figure 7. AC-Coupled CML

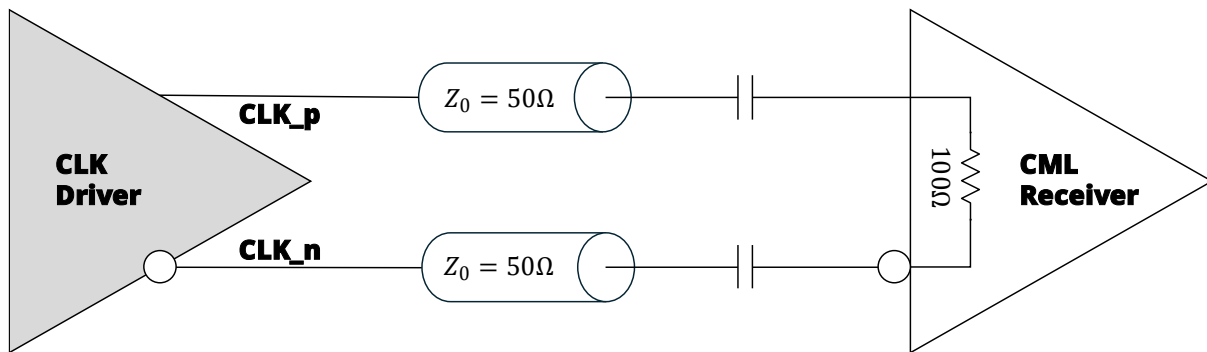


Figure 8. AC-Coupled CML (Receiver Termination)

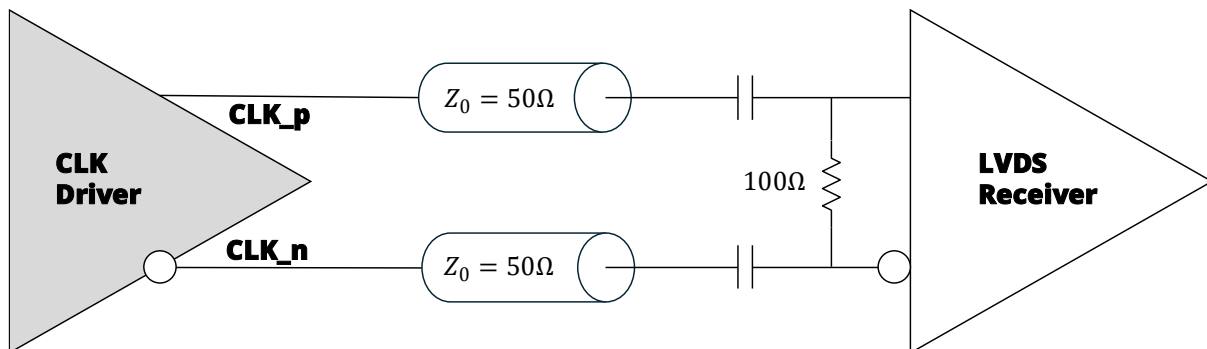


Figure 9. AC-Coupled LVDS

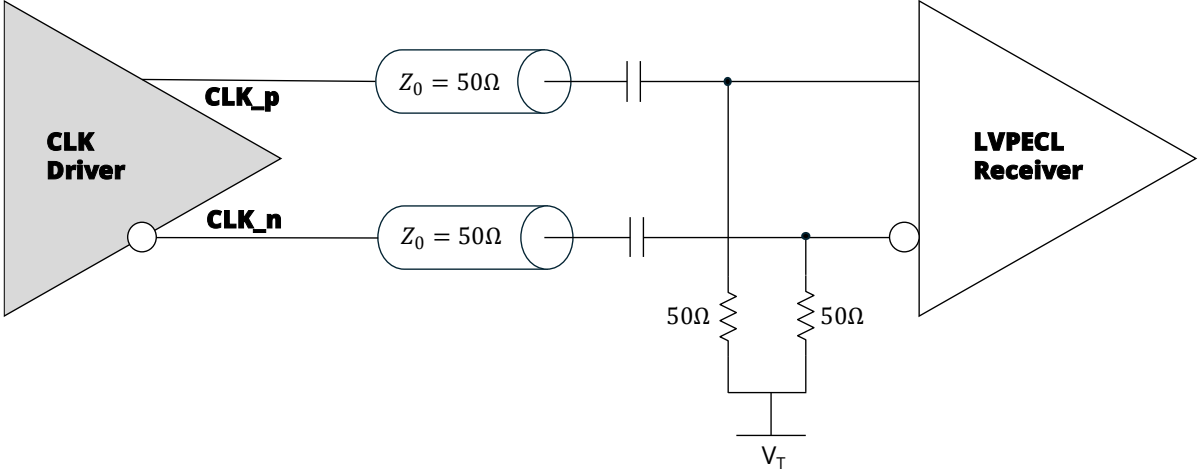


Figure 10. AC-Coupled LVPECL

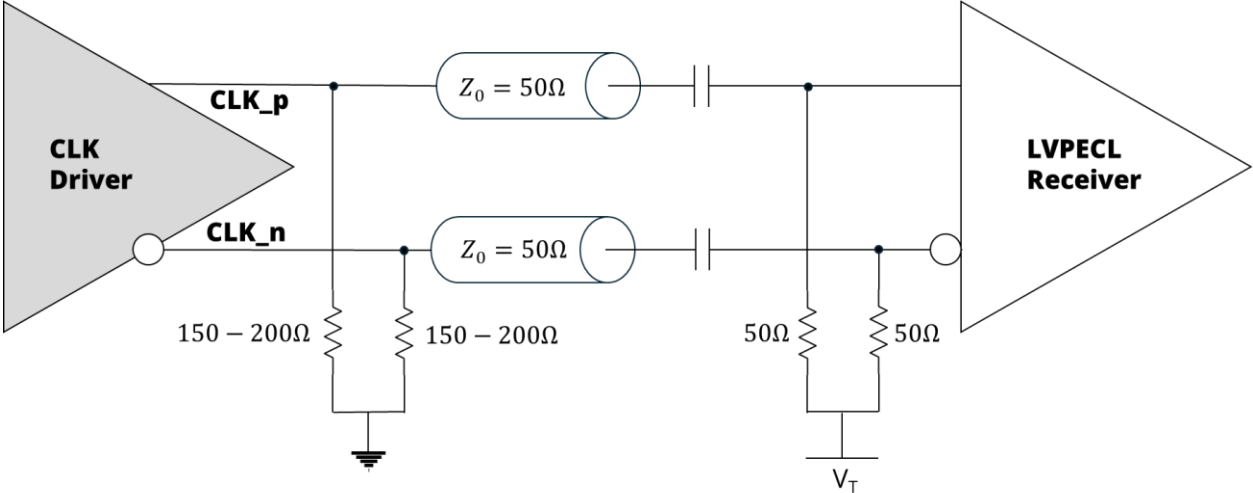


Figure 11. AC-Coupled LVPECL (DC Bias Resistor)

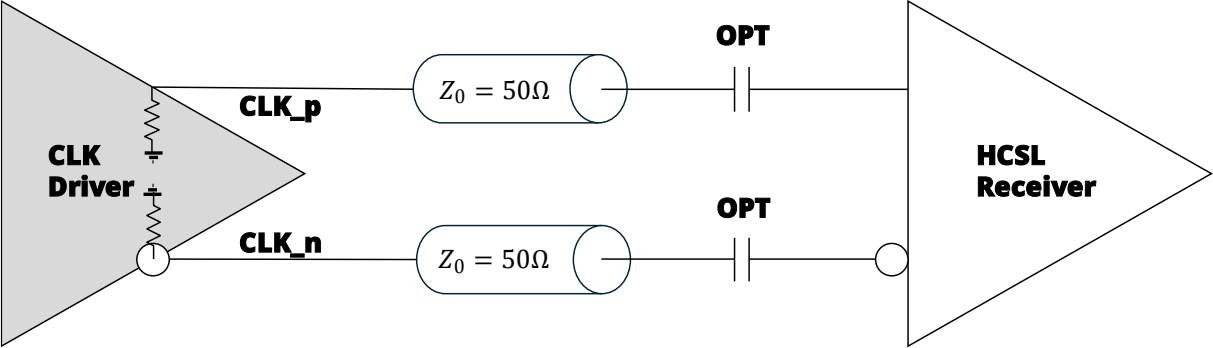


Figure 12. HCSL (Integrated Termination)

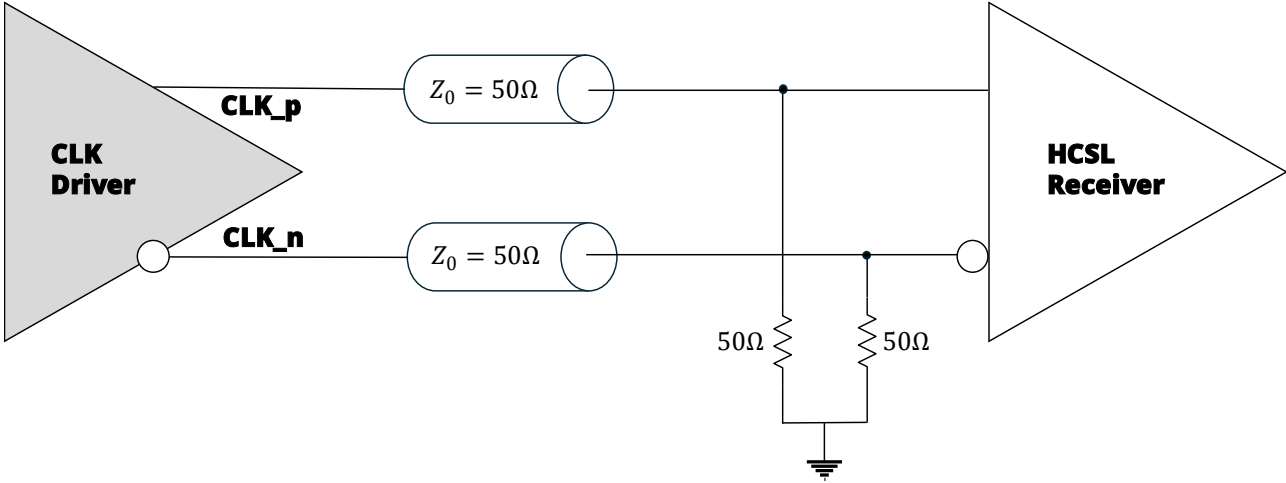


Figure 13. DC-Coupled HCSL (Receiver Termination)

# Output Timing

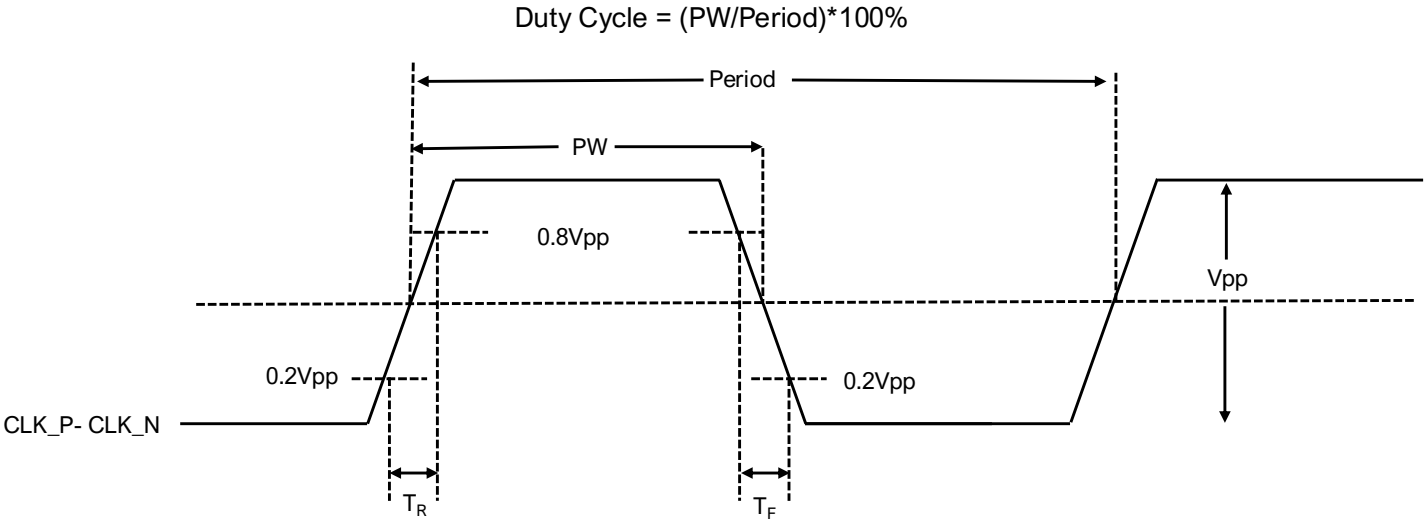


Figure 14. Output Timing across differential pair (CLK\_P-CLK\_N)

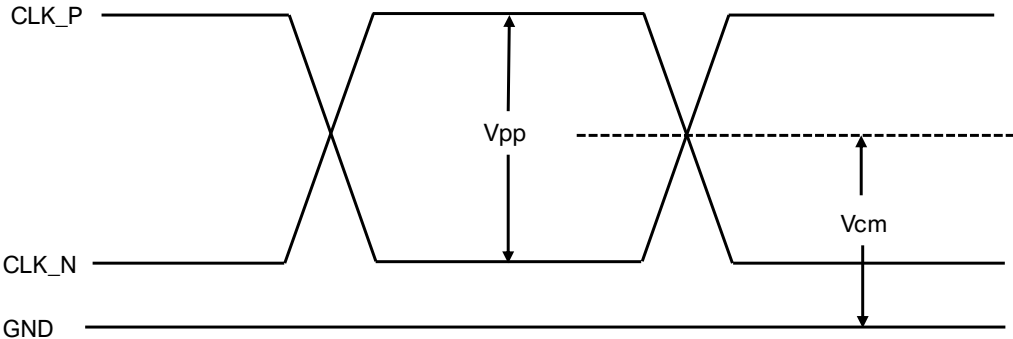


Figure 15. HCSL Output Level across differential pair (CLK\_P-CLK\_N)

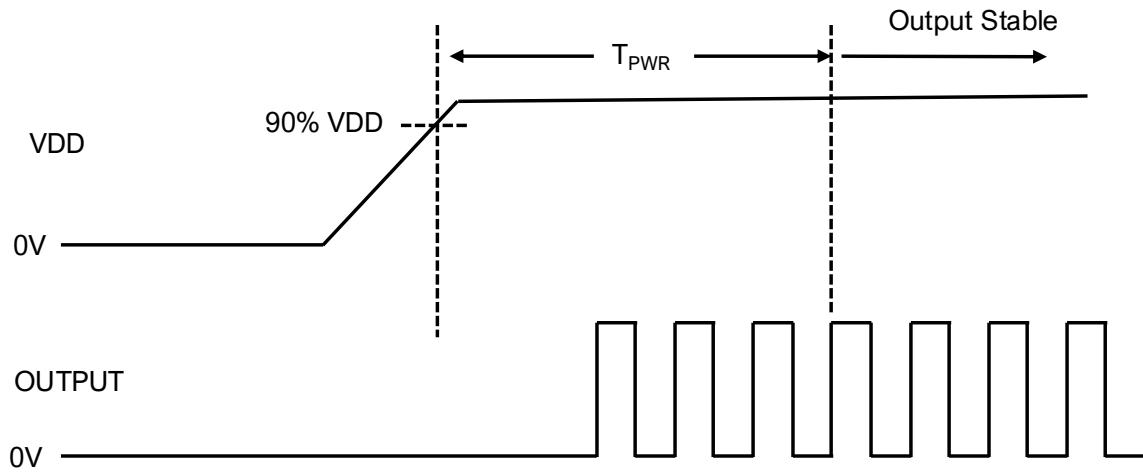


Figure 16. Powerup Timing

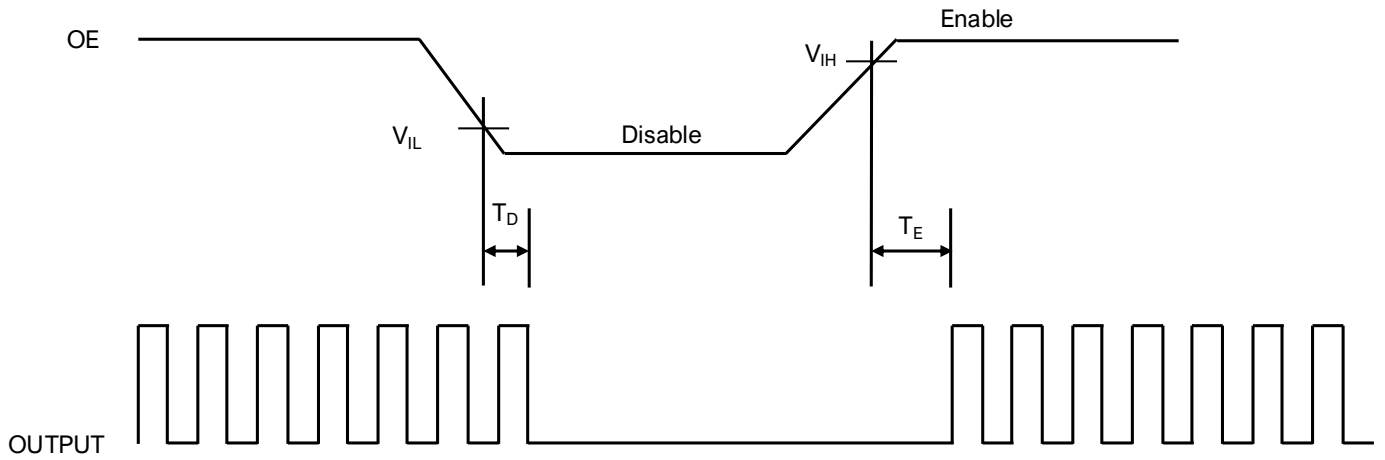


Figure 17. OE Enable/Disable Timing

## Packaging Information

Figure 18 shows the MS1220 packaging drawing.

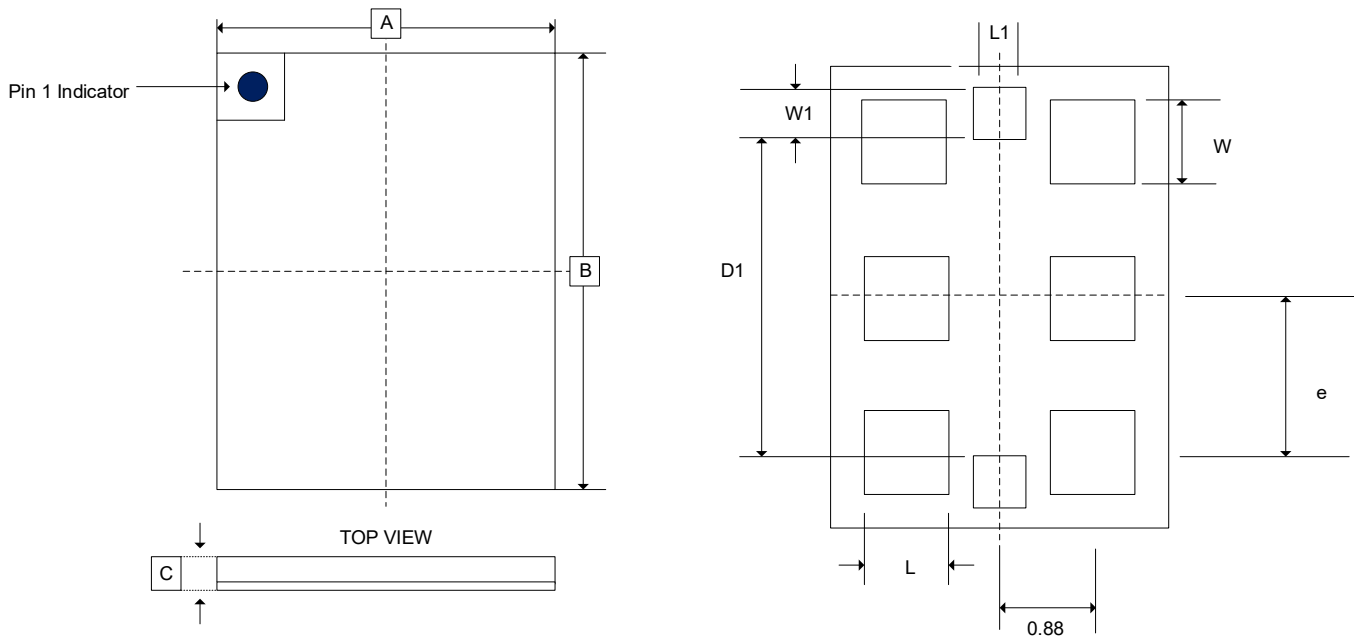


Figure 18. MS1220 Packaging Drawing (3.2mm x 2.5 mm)

Table 8. MS1220 Packaging Dimensions

Dimensions	Min	Nom	Max
A	2.5 BSC		
B	3.2 BSC		
C	1.246	1.346	1.446
W	0.55	0.6	0.65
L	0.5	0.55	0.6
W1	0.35	0.4	0.45
L1	0.35	0.4	0.45
e	1.1 BSC		
D1	2.2 BSC		
Package Edge Tolerance	0.1		
Mold Flatness	0.1		
Coplanarity	0.08		

Note: All dimensions are in millimeters

## Packaging Land Pattern

Figure 19 shows the MS1220 PCB land pattern.

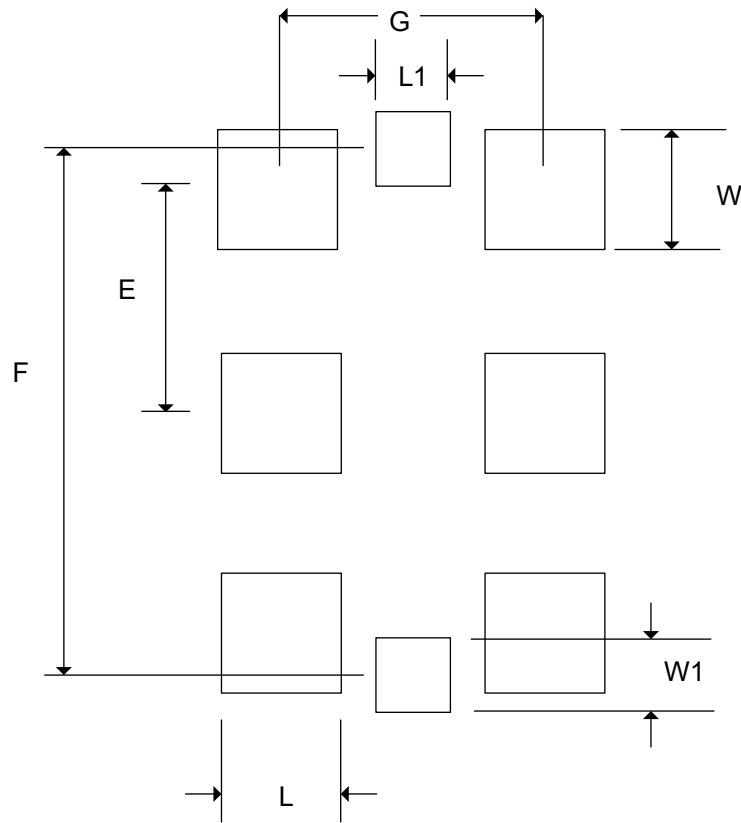


Figure 19. MS1220 Packaging Land Pattern Drawing (3.2mm x 2.5mm)

Table 9. MS1220 Packaging Land Pattern Dimensions

Dimensions	In mm
L	0.7
W	0.7
L1	0.5
W1	0.55
E	1.1
F	2.6
G	1.76

## Device Top Marking

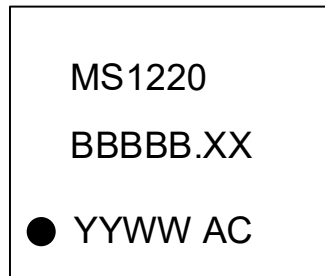


Figure 20. MS1220 Device Top Marking Showing Pin 1

Table 10. MS1220 Device Marking Legend

Line	Position	Description
1	1	Part Number
2	1-5	Wafer Lot Number
	6-7	Wafer #
3	Lot Traceability	
	1	Pin 1 Orientation Mark (Dot),
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	6-7	Assembly Code

### Part Ordering Information

Figure 21 shows a logic tree for ordering each of the three available parts.

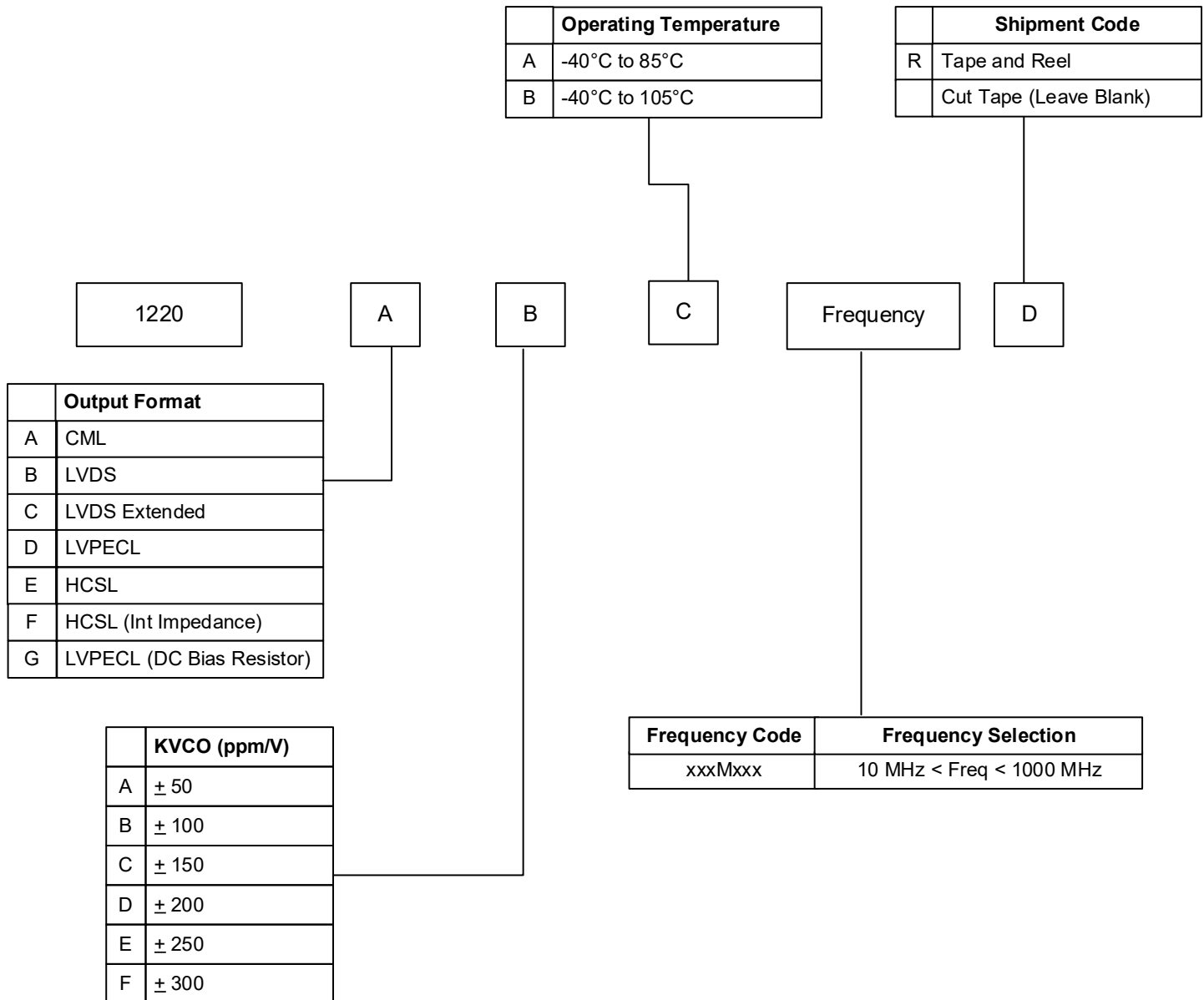


Figure 21. MS1220 Part Ordering Information

Table 11. Example of ordering part number

Base P/N	Output Format	KVCO (ppm/V)	Operating Temperature	Frequency Code	Shipment Type	Ordering part number
1220	LVDS	±150	-40°C to 85°C	312.5 MHz	Tape and Reel	<b>1220BCA312M500R</b>
1220	LVPECL	±50	-40°C to 105°C	625 MHz	Tape and Reel	<b>1220DAB625M000R</b>

### Reflow Profile (IPC/JEDEC-STD-020)

Figure 22 shows the reflow profile for MS1220

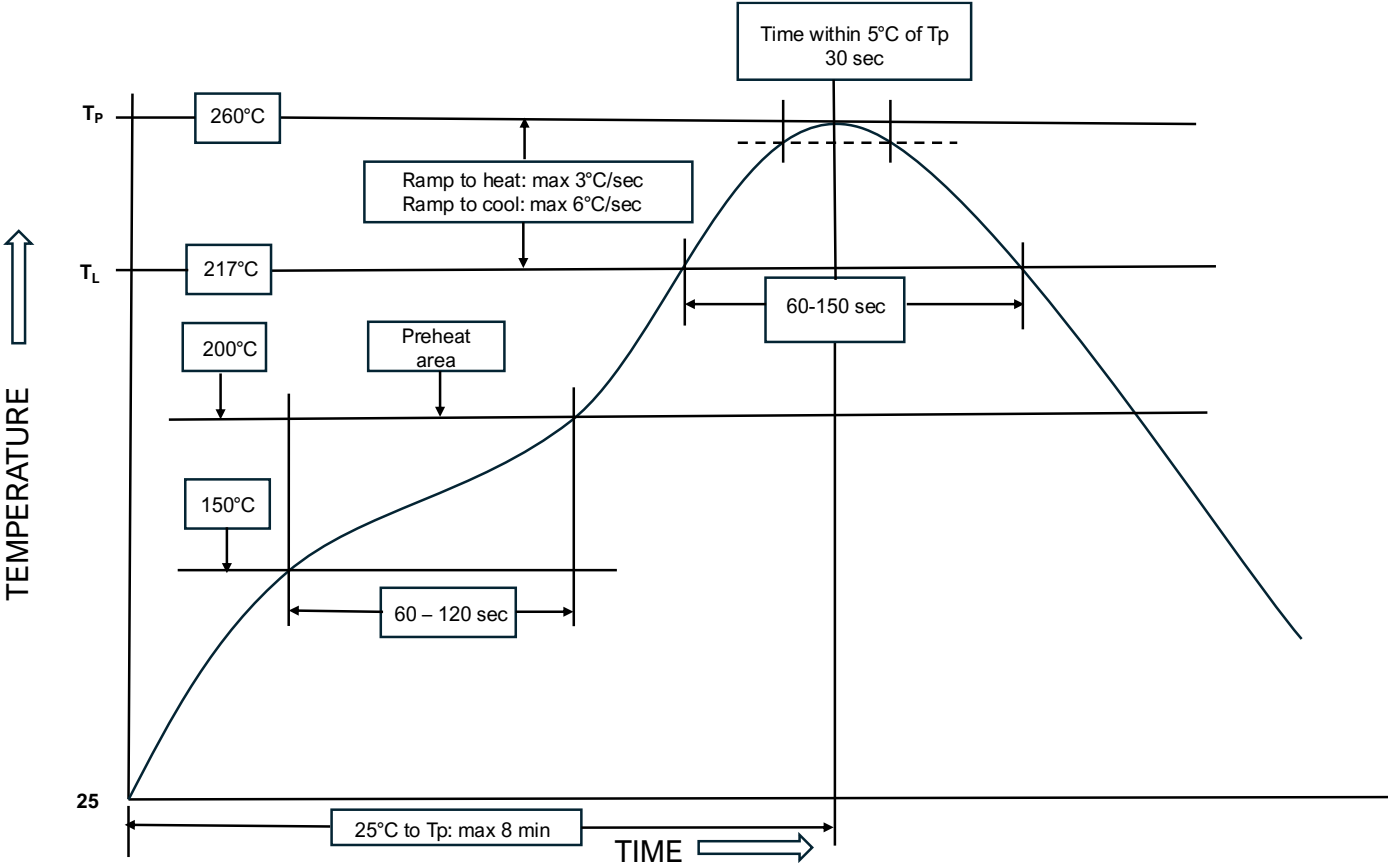


Figure 22. MS1220 Reflow Profile

## REVISION HISTORY

### Revision 1.3

April 20, 2026

- Added LVPECL Load Termination
- Updated Phase Noise Plots
- Updated ordering part number (include LVPECL Load Termination)

### Revision 1.2

October 17, 2025

- Updated Figure 13: Output Driver (HCSL); removed AC coupling
- Updated ordering part number

### Revision 1.1

September 2, 2025

- Added Timing Diagram
- Updated Output Driver information (LVPECL, HCSL)
- Added Reflow Profile

### Revision 1.0

December 20, 2024

- Initial Release

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