

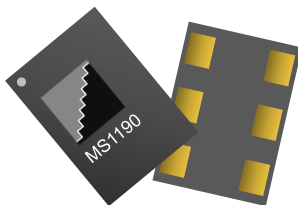
## Ultra-Low Jitter Crystal Oscillators (XO)

### Features

- Available at any frequency from 20 MHz to 2200 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 21.8 fs at 312.50 MHz
  - 21.6 fs at 491.52 MHz
  - 19.6 fs at 625 MHz
  - 21.7 fs at 1250 MHz
  - 18.8 fs at 1600 MHz
- Total stability of  $\pm 20$  ppm
- CML/LVDS/LVDS-EXT/LVPECL/HCSL output formats
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jump
- Industry standard 2.0X1.6mm 6-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range -40°C to 85°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

### Applications

- Network Equipment (Optical Modules, routers)
- 100G/200G/400G/800G OTN, Coherent optics
- Storage, switches, servers, NICs, accelerators
- Datacenter
- 3G to 24G SDI broadcast video
- 10G/40G/100G optical ethernet
- 56G/112G PAM4 Clocking
- Test and measurement equipment



### General Description

The MS1190 is a crystal oscillator (XO) powered by our Virtual Crystal™ technology that enables very stable fully programmable multi-GHz clocks with extremely low phase noise.

Adaptive fully autonomous DSP algorithms running in the background continuously monitor and ensure robust and consistent performance over process, voltage and temperature variations.

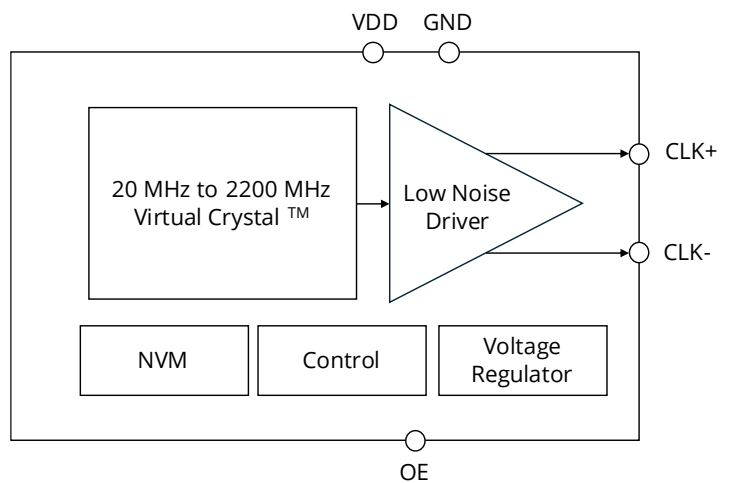
The devices are factory programmed to provide any frequency between 20 MHz and 2200 MHz with less than 1 ppb resolution.

The MS1190 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

### Device Information

Part Number	Package	Description
MS1190	2.0X1.6mm 6-pin LGA	XO

Figure 1. Functional Block Diagram



# MS1190

## Pin Assignment and Pin Description

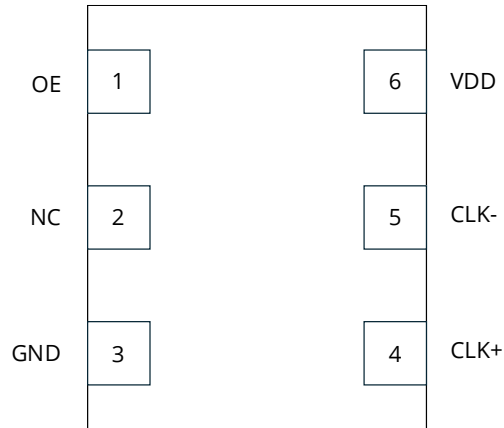


Figure 2. MS1190 Pin Assignments

Table 1. MS1190 Pin Descriptions

Pin No	Name	Description
1	OE	Output Enable
2	NC	No Connect
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply

## Specifications

**Table 2. Electrical Specifications**

Typical values are specified at  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = 1.8\text{V}$  unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination. A 0.1 $\mu\text{F}$  and 10 $\mu\text{F}$  bypass capacitor should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
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### Frequency Range

Frequency Range	$F_{CLK}$	All Output Formats	20		2200	MHz
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### Frequency Stability

Frequency Stability*	$F_{STB}$	$-40^\circ\text{C}$ to $85^\circ\text{C}$	-20		20	PPM
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\*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year,  $+25^\circ\text{C}$ ). Aging is estimated from environmental reliability tests;

### Clock Output Jitter Characteristics

RMS Phase Jitter (12 KHz – 20 MHz)	$\Phi_{JITTER}$	Frequency= 491.52 MHz		21.6	32	fs
		Frequency= 625 MHz		19.6	30	

**Note:**

Phase jitter measured on Agilent 5052B Signal Source Analyzer

### Operating Voltage/Temperature Range

Supply Voltage	$V_{DD}$		1.71	1.8	1.89	V
Temperature Range	$T_A$	Industrial Temperature	-40		85	$^\circ\text{C}$

## Current Consumption

Supply Current	$I_{DD}$	LVDS Output (Output Enabled)	150	180	mA
		All Other Outputs (Output Enabled)	160	190	mA
		Tristate Hi-Z (Output Disabled)	70	84	mA

## Input Characteristics

Digital Input Levels (OE)	$V_{IH}$		$0.7XV_{DD}$			V
	$V_{IL}$				$0.3XV_{DD}$	V
Output Enable (OE)	$T_D$	Output Disable Time			3	us
	$T_E$	Output Enable Time			20	us
Powerup Time	$T_{PWR}$	Time from $0.9xV_{DD}$ until output frequency ( $F_{CLK}$ ) within spec			10	ms

## PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (312.5MHz)		-114		dBc
Power Supply-Jitter Sensitivity	PSJS			0.1		fs/mv

**Note:**

(1) Measured with 50 mVpp ripple from 50 KHz to 1 MHz applied on VDD Pin

## Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% $V_{PP}$ )	$T_R / T_F$	All Output Formats		65	100	ps
LVDS Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	0.5	0.7	0.9	V
LVDS Extended Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	0.8	1.2	1.6	V
CML Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	0.6	0.8	1	V
LVPECL Output (AC Mode)	$V_{pp}$	Differential Pk-Pk	1.2	1.4	1.6	V
HCSL Output	$V_{pp}$	Differential Pk-Pk	1.1	1.35	1.6	V
HCSL Output Voltage	$V_{CM}$	Common Mode Voltage	340	350	360	mV

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		85	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C

**Note:** Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.

**Table 4. Environmental Compliance**

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Moisture Sensitivity Level (MSL)	3
Note: For additional information not listed, please contact Mixed-Signal Devices.	

**Table 5. ESD Levels**

Description	Description	Specification	Level
HBM <sup>1</sup>	Human Body Model	JEDEC JS-001	2000V
CDM <sup>2</sup>	Charge Device Model	JEDEC JESD22-C101	500V
<b>Notes:</b> 1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155 2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157			

**Table 6. Package Thermal Information**

Package	Parameter	Symbol	Value	Unit
2.0mmx1.6mm 6 pin LGA	Thermal Resistance, Junction to Ambient	$\theta_{JA}$	110	°C/W
	Thermal Resistance, Junction to Board	$\theta_{JB}$	60	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	$T_J$	125	°C
<b>Note:</b> The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

**Table 7. Typical Output Phase Noise Characteristics**

VDD= 1.8V, T<sub>A</sub>= 25°C, Output Type = LVDS-EXT.

Offset frequency	312.5 MHz	491.52 MHz	625 MHz	1250 MHz	1600 MHz	Unit
1 KHz	-103	-98	-99	-93	-91	dBc/Hz
10 KHz	-132	-130	-127	-122	-119	dBc/Hz
100 KHz	-154	-152	-149	-143	-142	dBc/Hz
1 MHz	-164	-160	-159	-152	-152	dBc/Hz
10 MHz	-165	-161	-160	-151	-152	dBc/Hz
20 MHz	-166	-161	-160	-153	-152	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	21.8	21.6	19.6	21.7	18.8	fs

### Typical Output Measured Phase Noise Plots

This section shows MS1190 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type =LVDS-EXT.

The plots were captured using an Agilent E5052B Signal Source Analyzer.

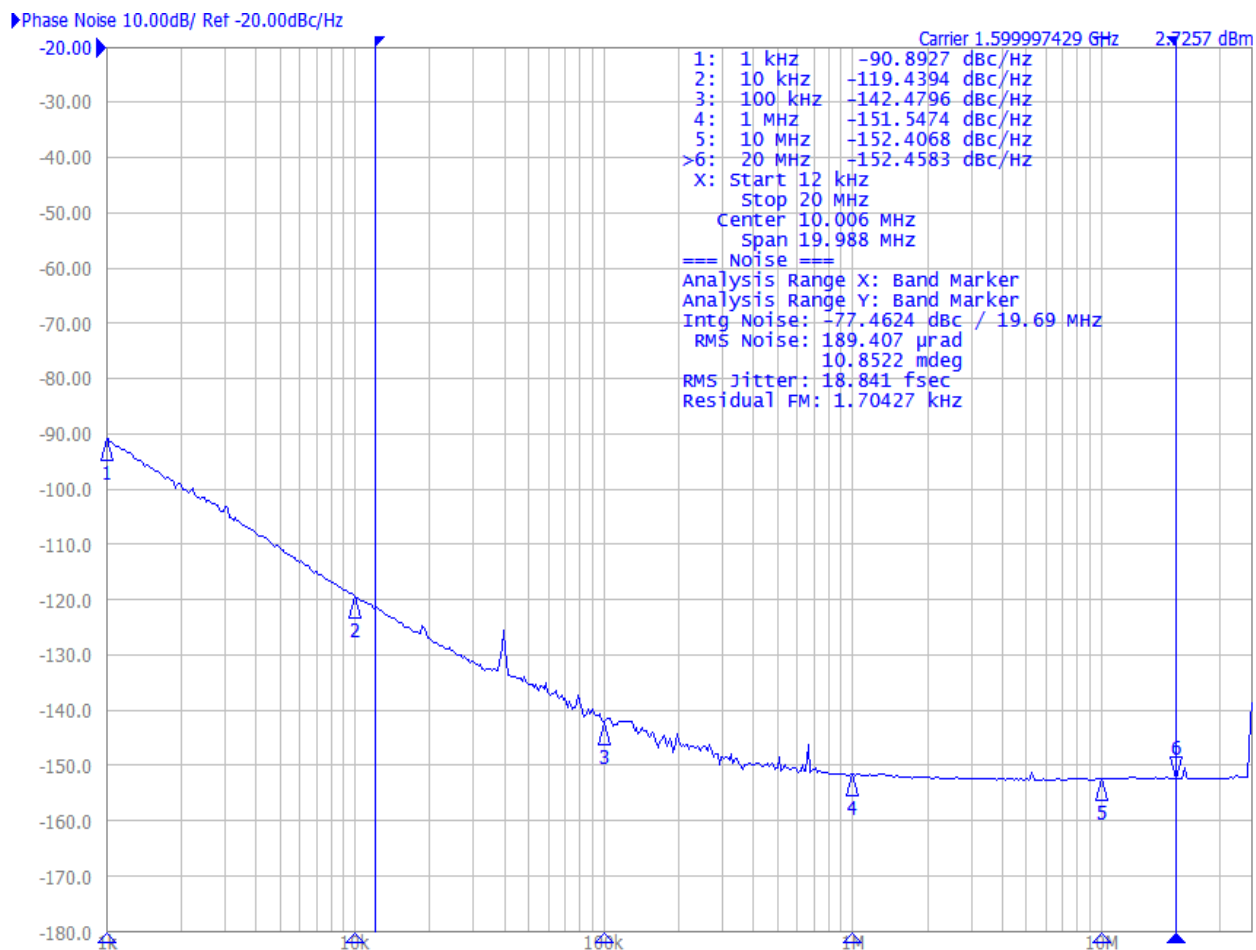


Figure 3. Carrier: 1600 MHz

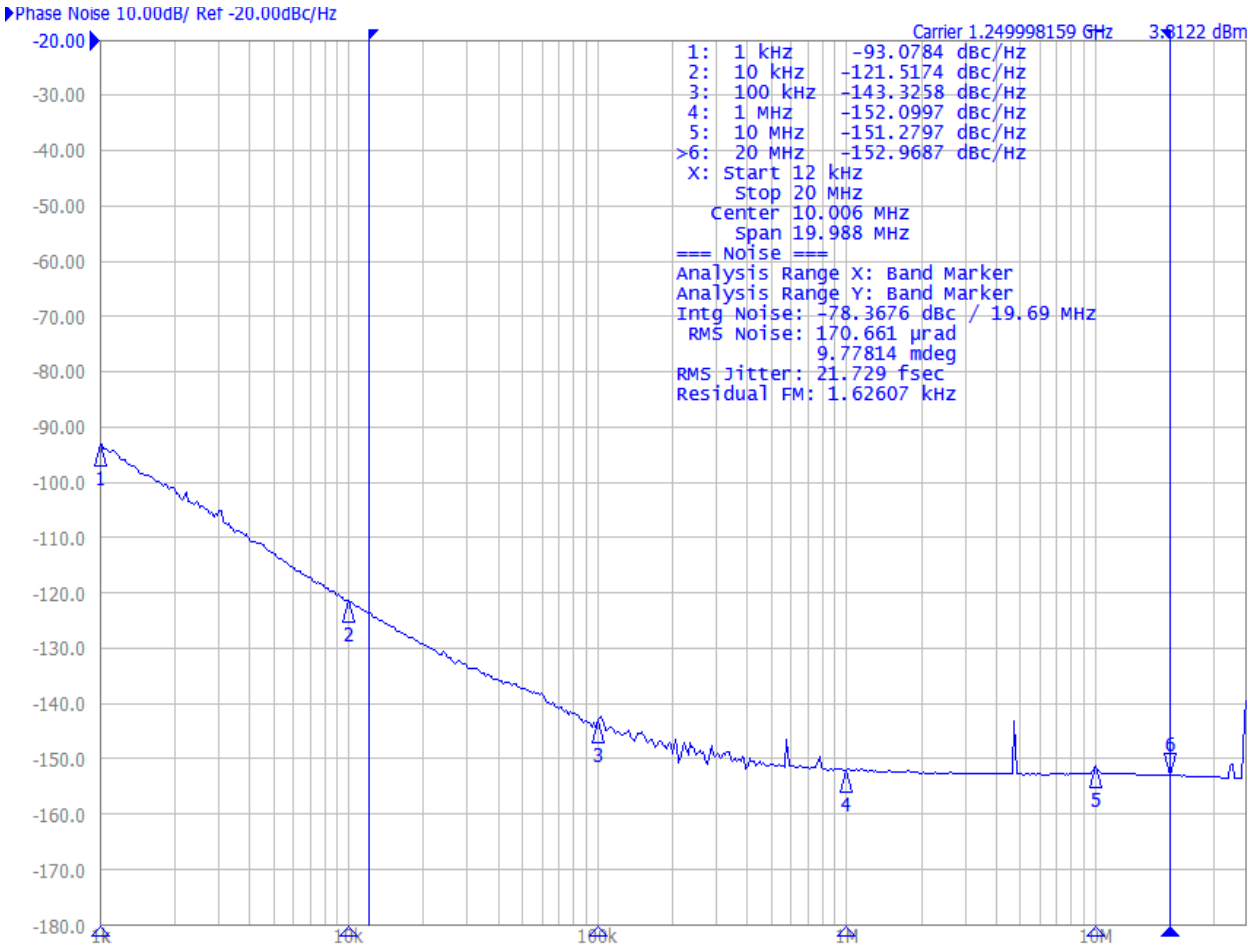


Figure 4. Carrier: 1250 MHz

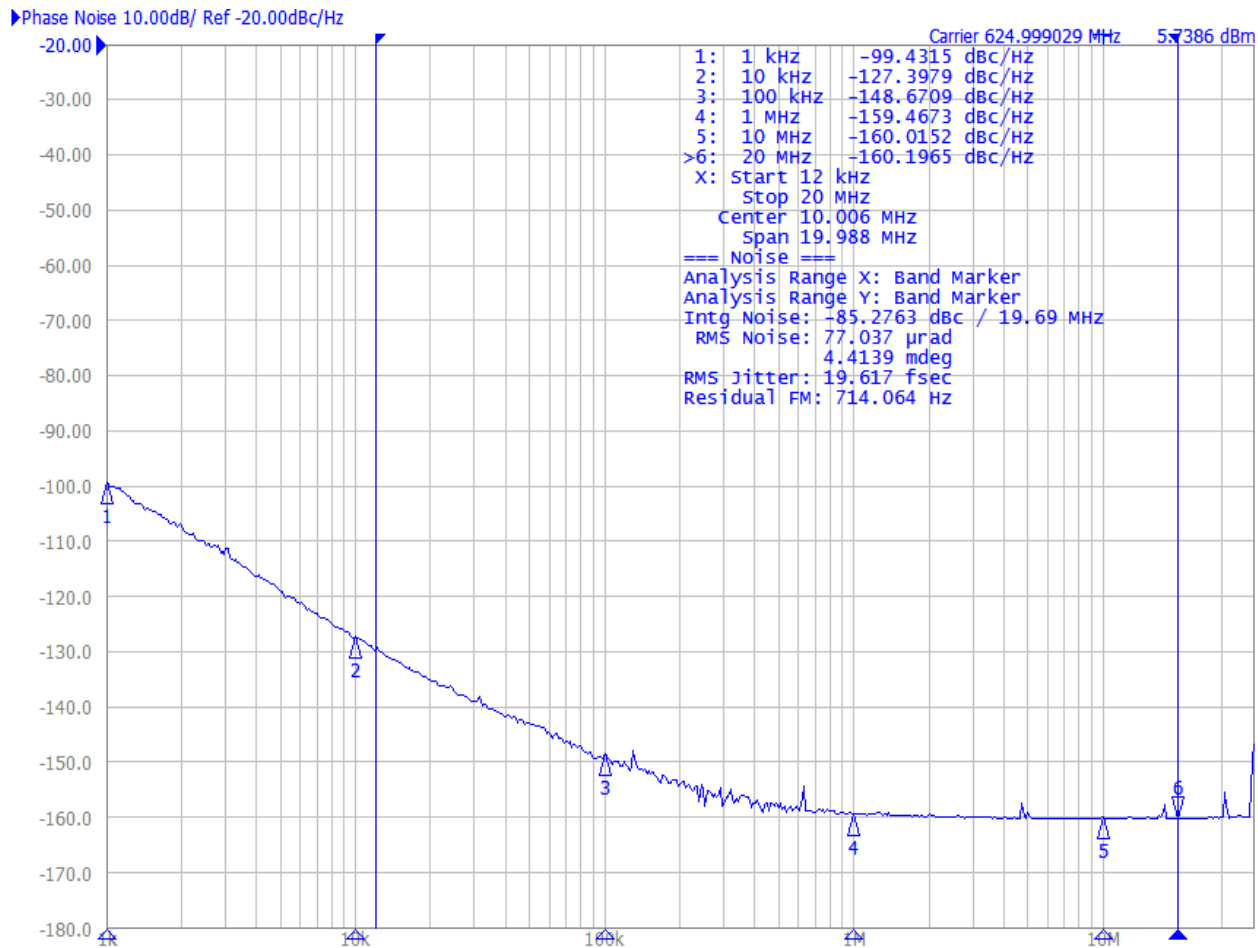


Figure 5. Carrier: 625 MHz

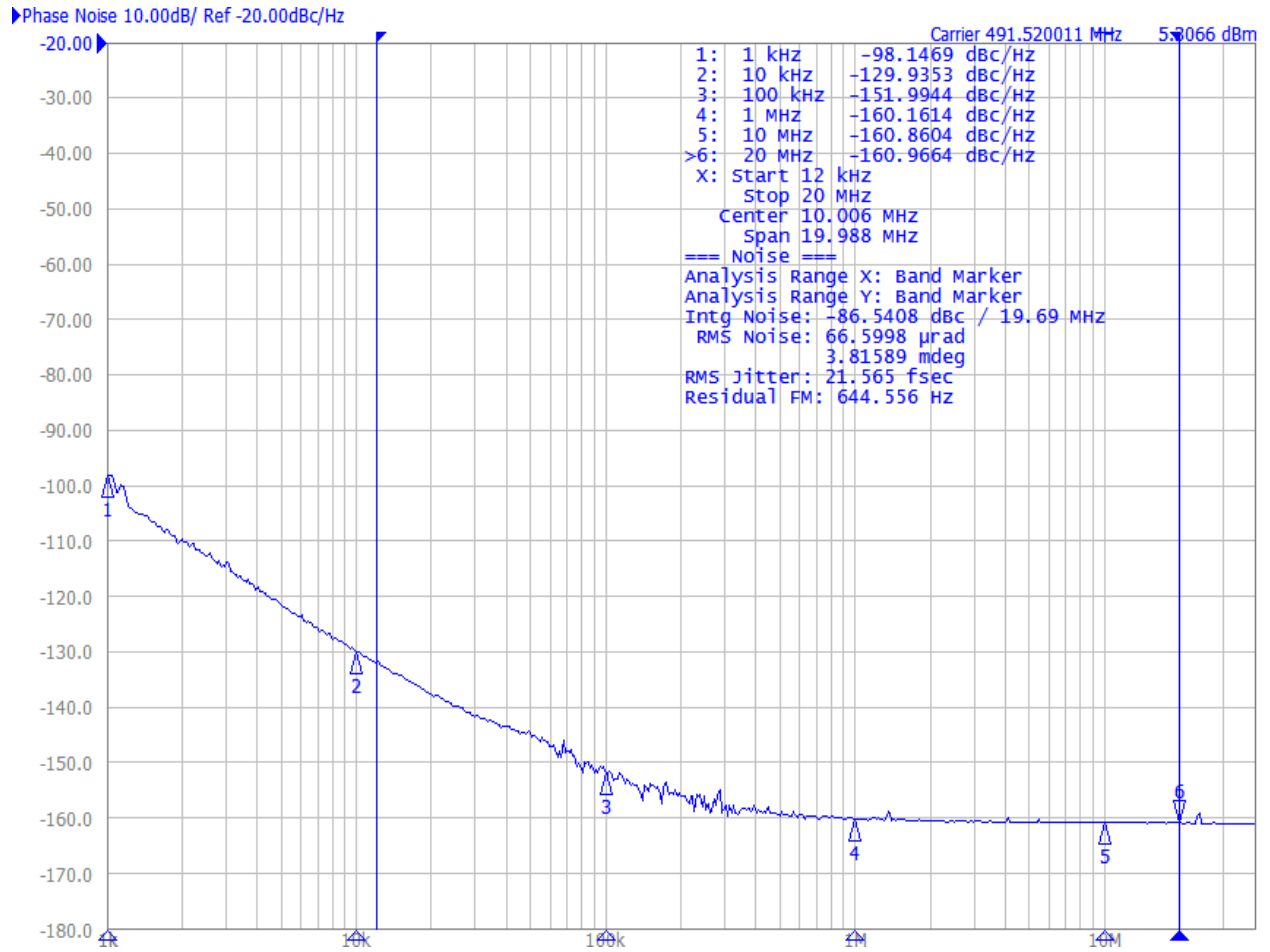


Figure 6. Carrier: 491.52 MHz

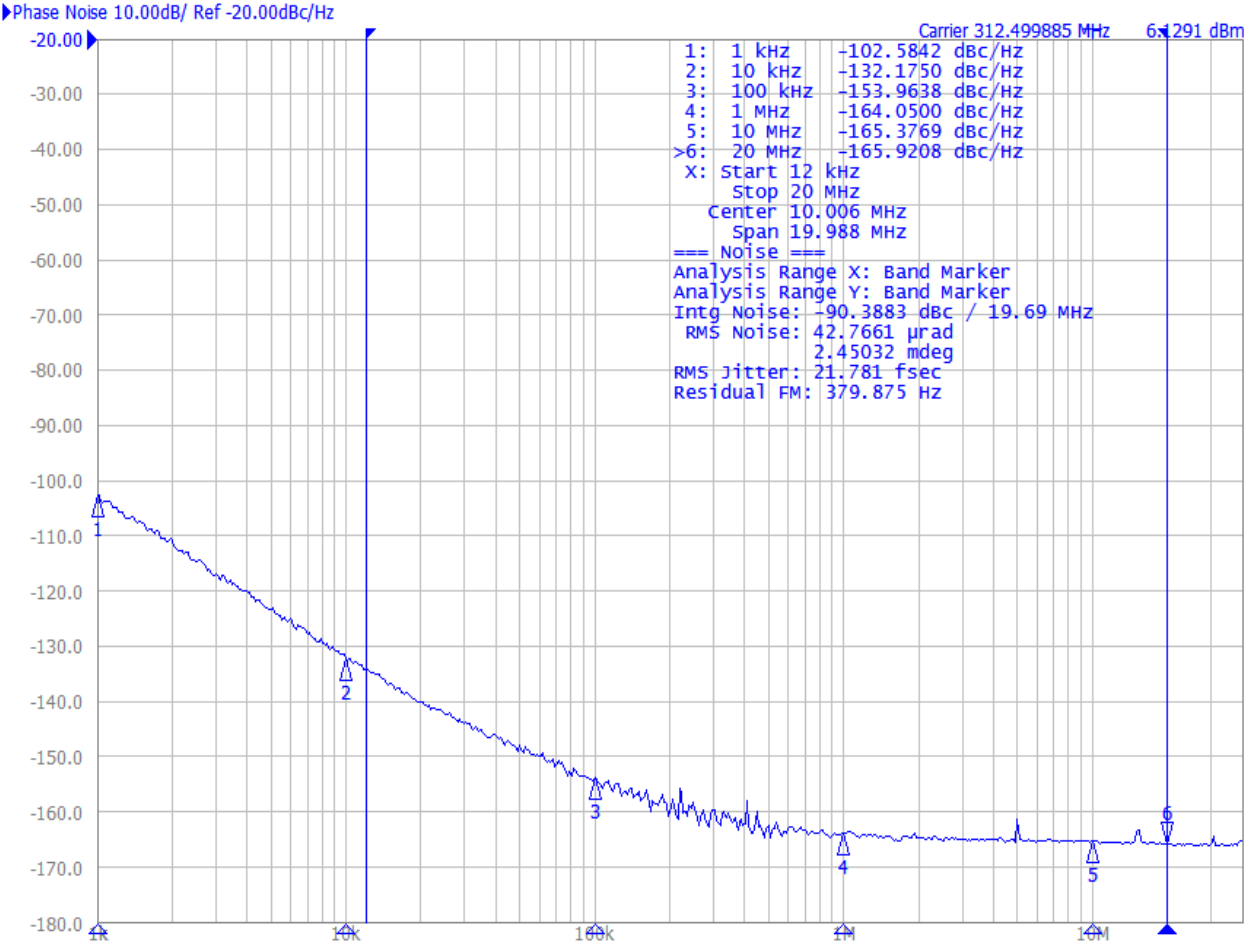


Figure 7. Carrier: 312.5 MHz

## Output Terminations

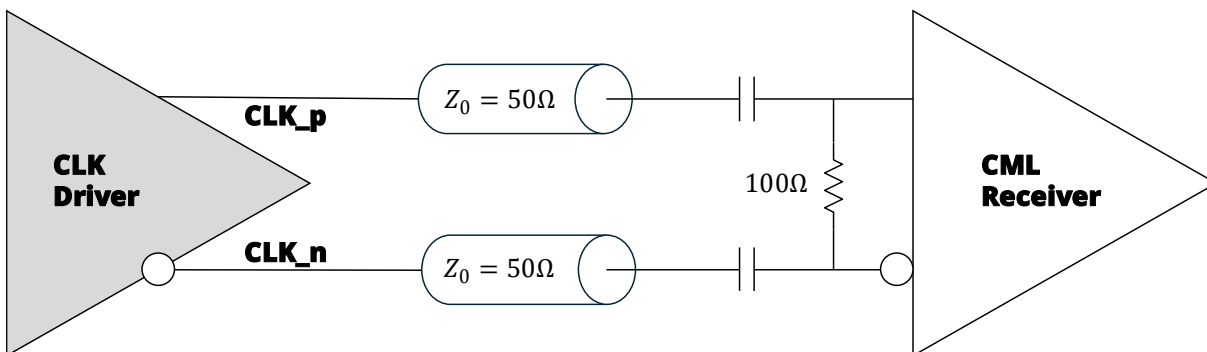


Figure 8. AC-Coupled CML

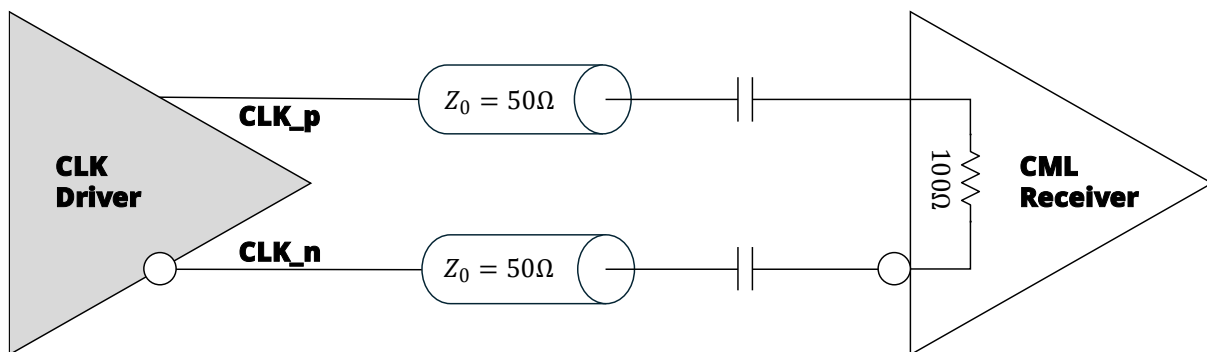


Figure 9. AC-Coupled CML (Receiver Termination)

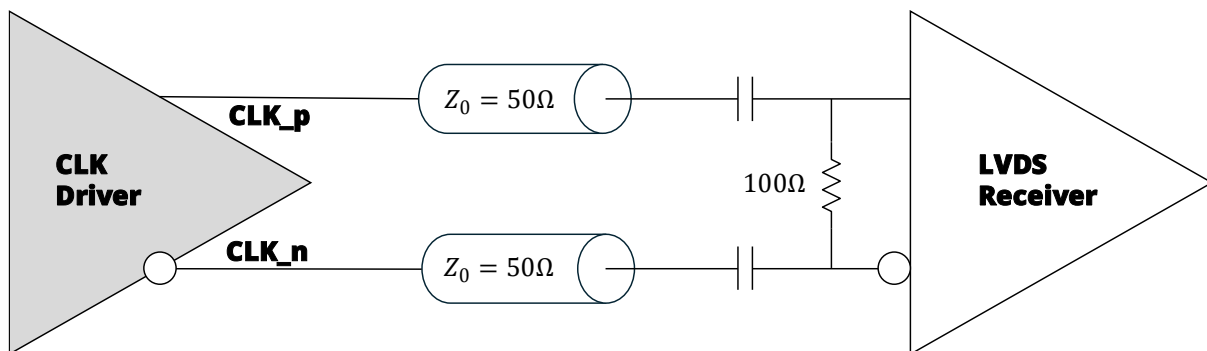


Figure 10. AC-Coupled LVDS

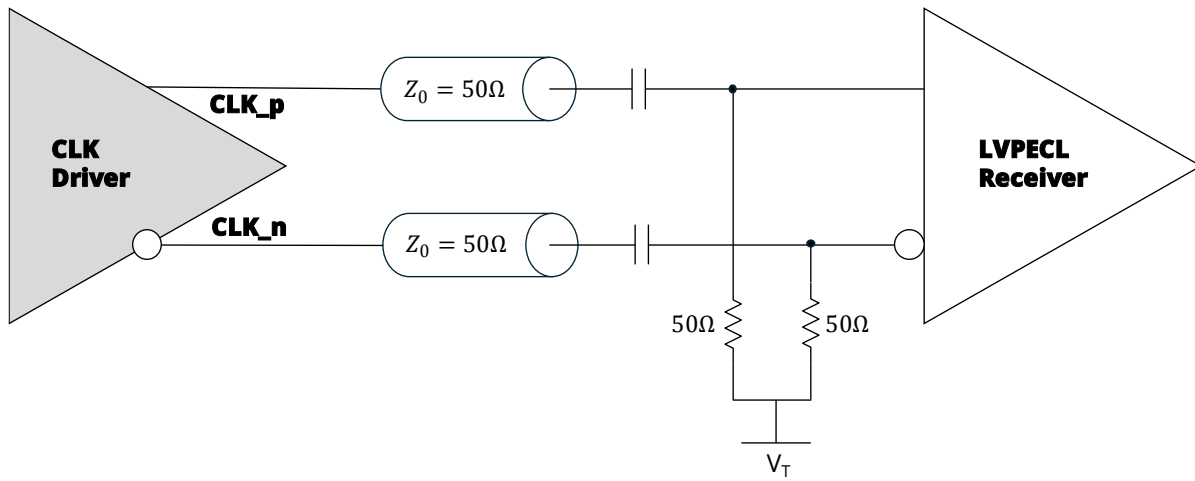


Figure 11. AC-Coupled LVPECL

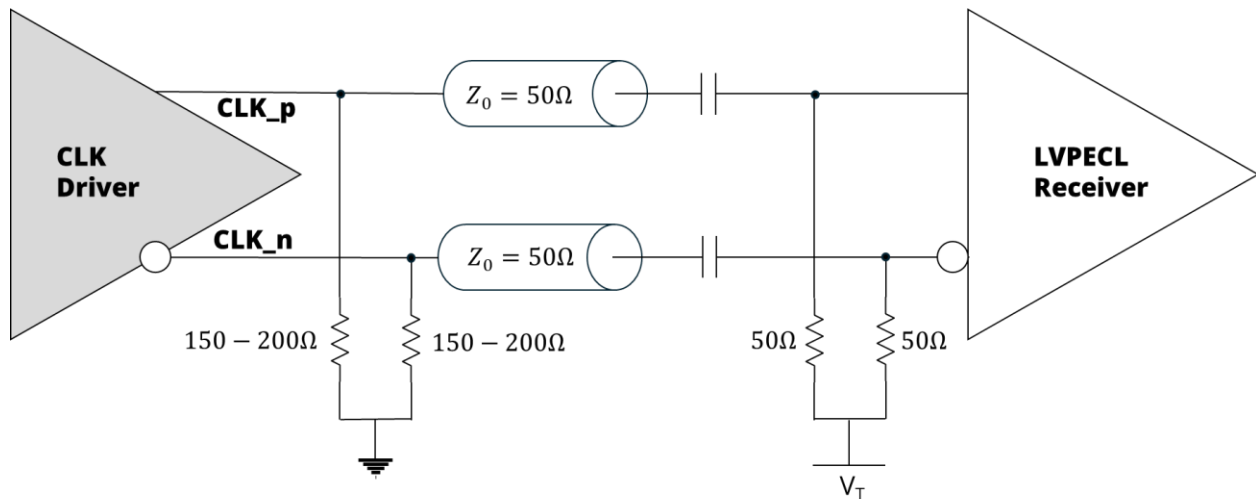


Figure 12. AC-Coupled LVPECL (DC Bias Resistor)

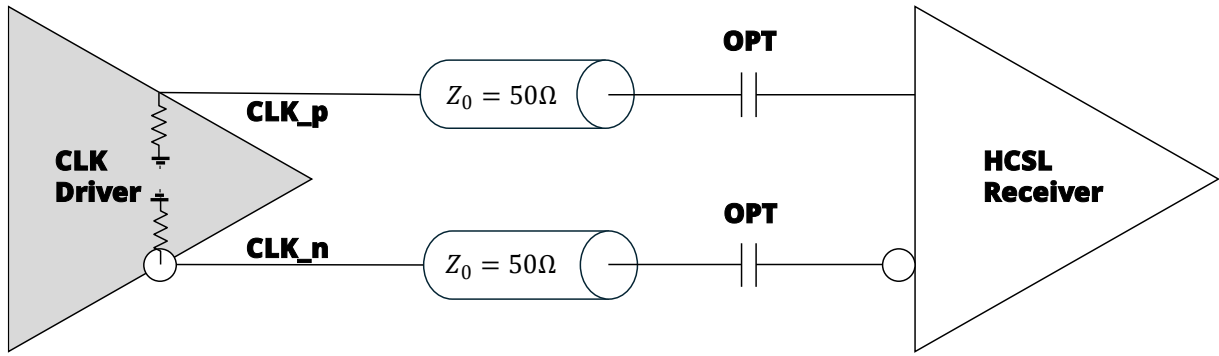


Figure 13. HCSL (Integrated Termination)

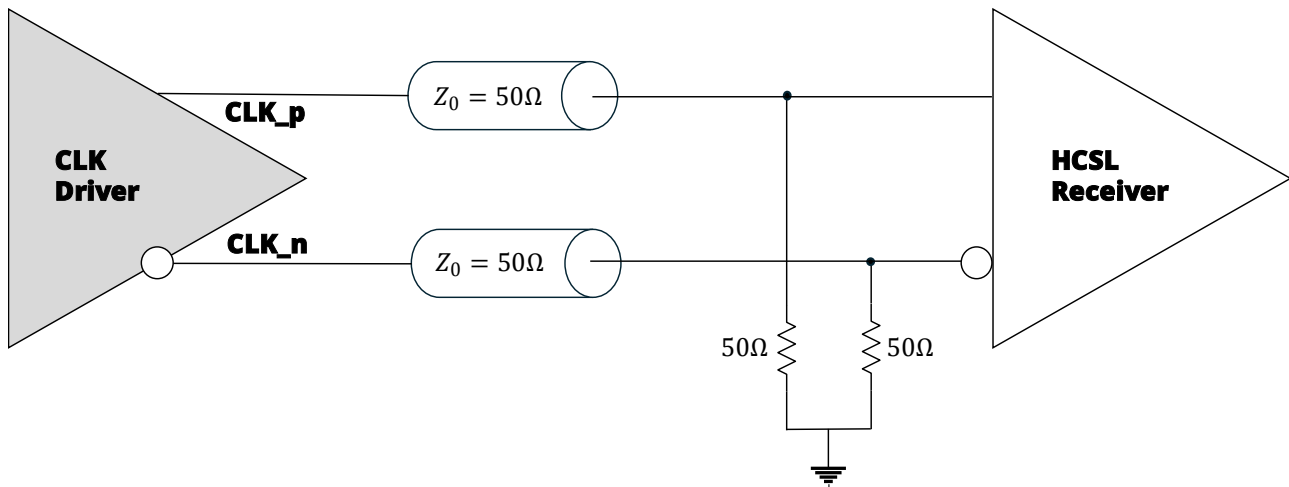


Figure 14. DC-Coupled HCSL (Receiver Termination)

# Output Timing

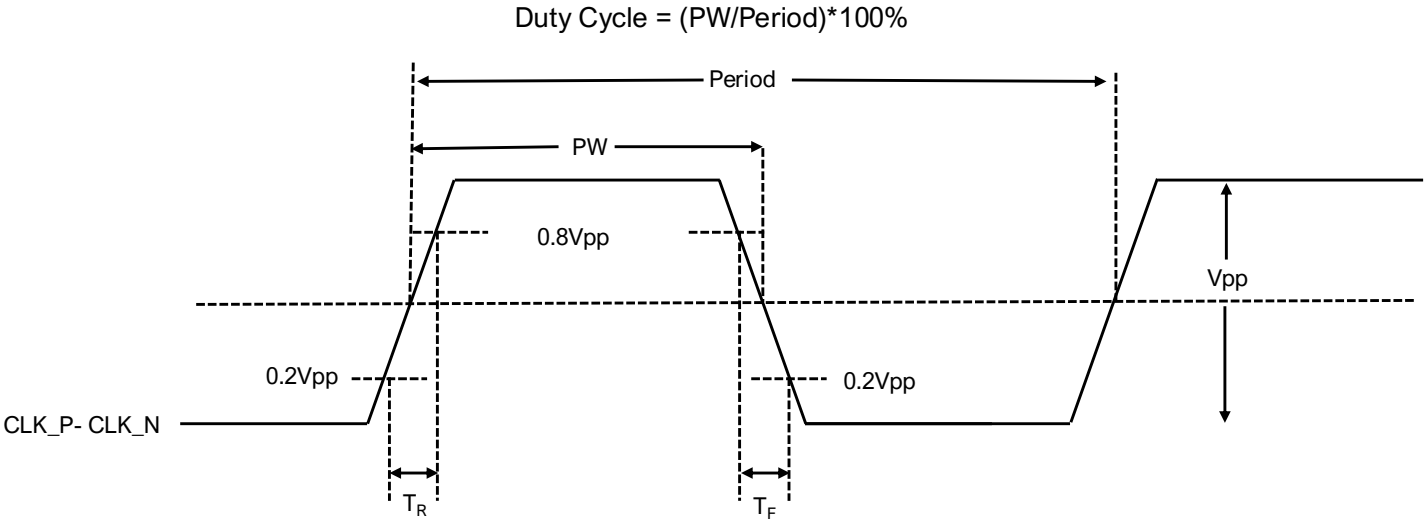


Figure 15. Output Timing across differential pair (CLK\_P-CLK\_N)

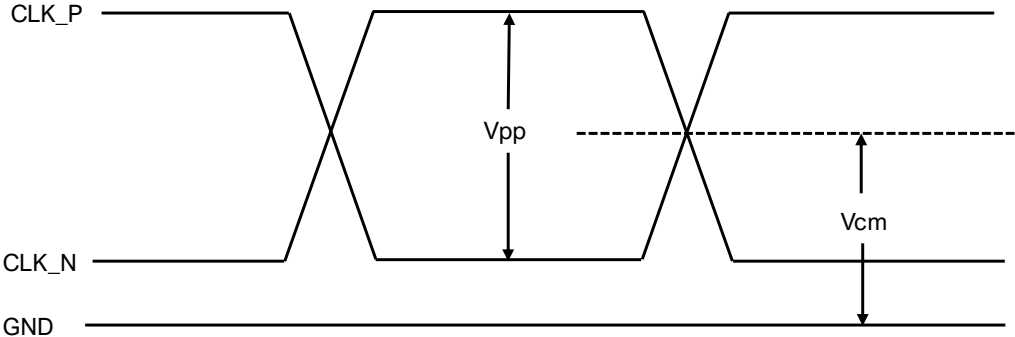


Figure 16. HCSL Output Level across differential pair (CLK\_P-CLK\_N)

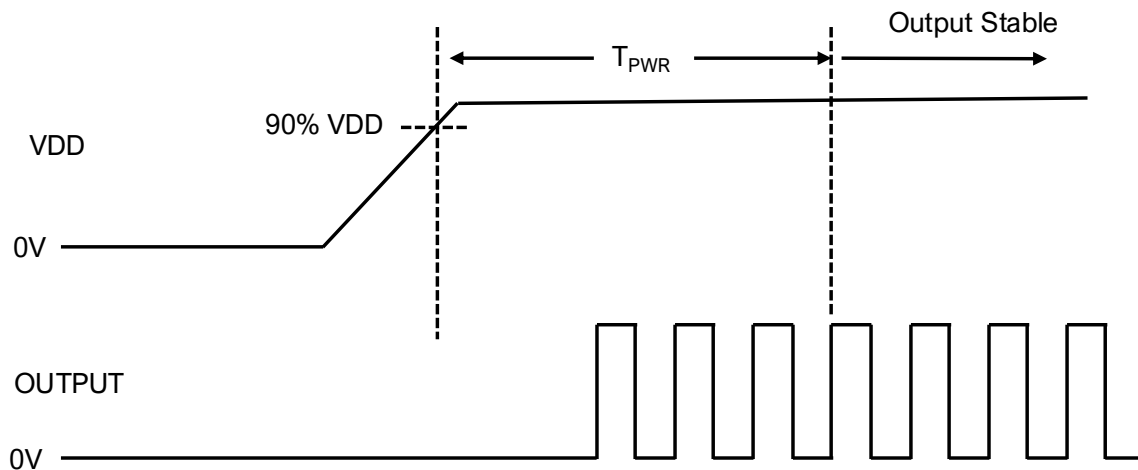


Figure 17. Powerup Timing

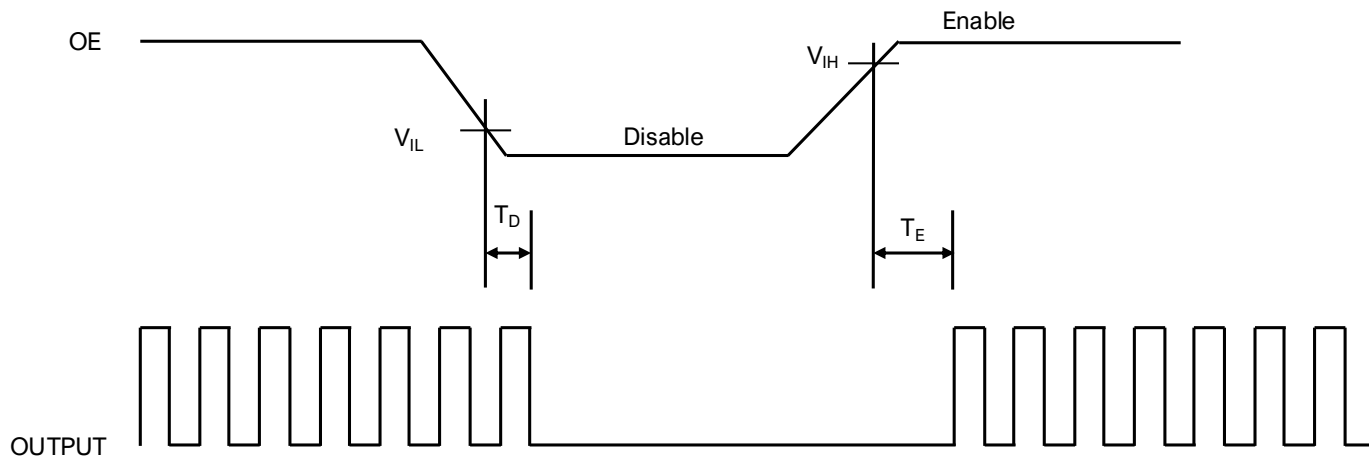


Figure 18. OE Enable/Disable Timing

## Packaging Information

Figure 19 shows the MS1190 packaging drawing.

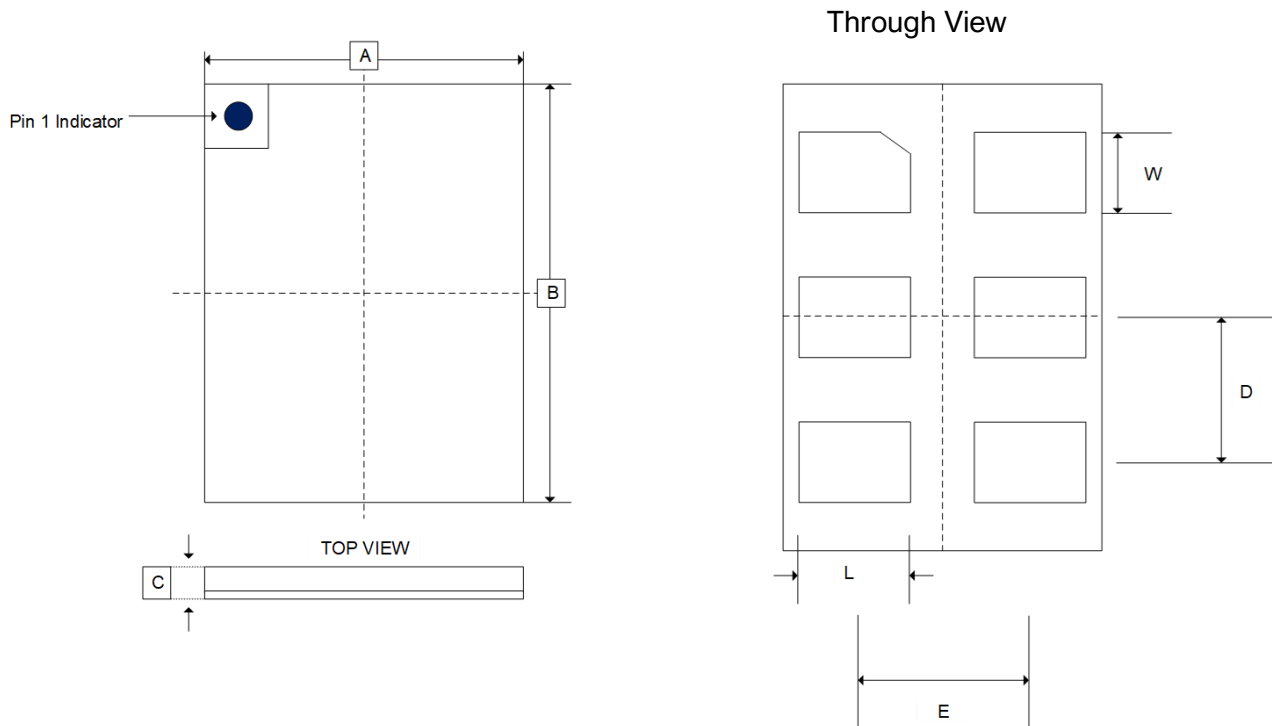


Figure 19. MS1190 Packaging Drawing (2.0X1.6 mm)

Table 8. MS1190 Packaging Dimensions

Dimensions	Min	Nom	Max
A	1.6 BSC		
B	2.0 BSC		
C	1.246	1.346	1.446
L	0.5	0.5	0.5
W	0.35	0.35	0.35
D	0.75 BSC		
E	0.95 BSC		
Package Edge Tolerance	0.1		
Mold Flatness	0.1		
Coplanarity	0.08		

Note: All dimensions are in millimeters

## Packaging Land Pattern

Figure 20 shows the MS1190 PCB land pattern.

Note: All dimensions are in millimeters

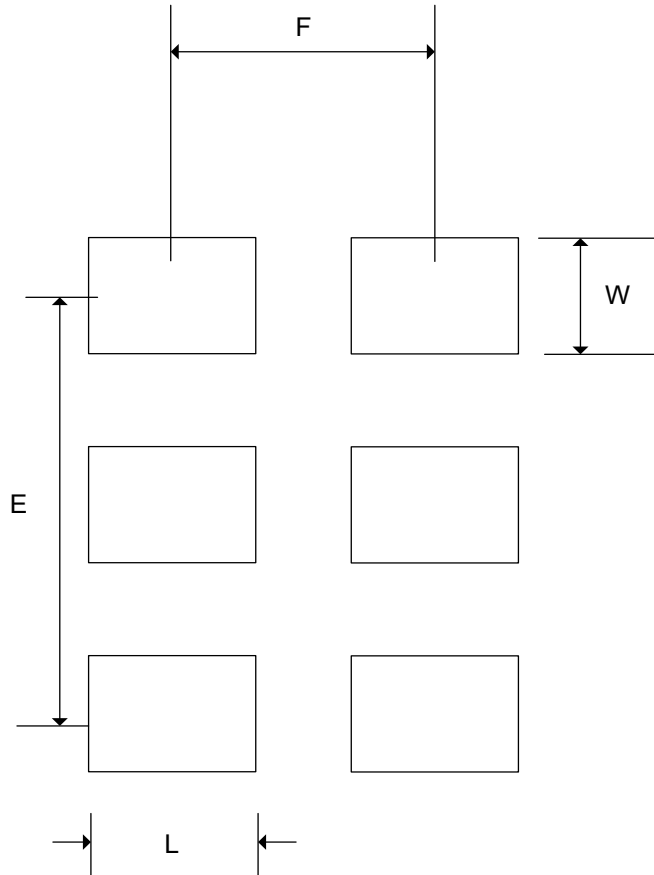


Figure 20. MS1190 Packaging Land Pattern Drawing (2.0X1.6 mm)

Table 9. MS1190 Packaging Land Pattern Dimensions

Dimensions	Length
L	0.80
W	0.524
E	1.564
F	1.15

Device Top Marking

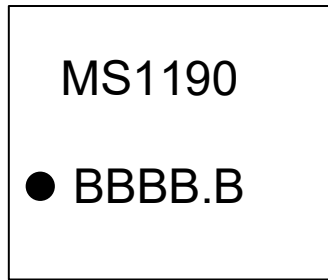


Figure 21. MS1190 Device Top Marking Showing Pin 1

Table 10. MS1190 Device Marking Legend

Line	Position	Description
1	1	Product Marking
2	1	Pin 1 Orientation Mark (Dot)
	2-5	Lot Number
	6	Wafer Number

## Part Ordering Information

Figure 22 shows a logic tree for ordering each of the available parts.

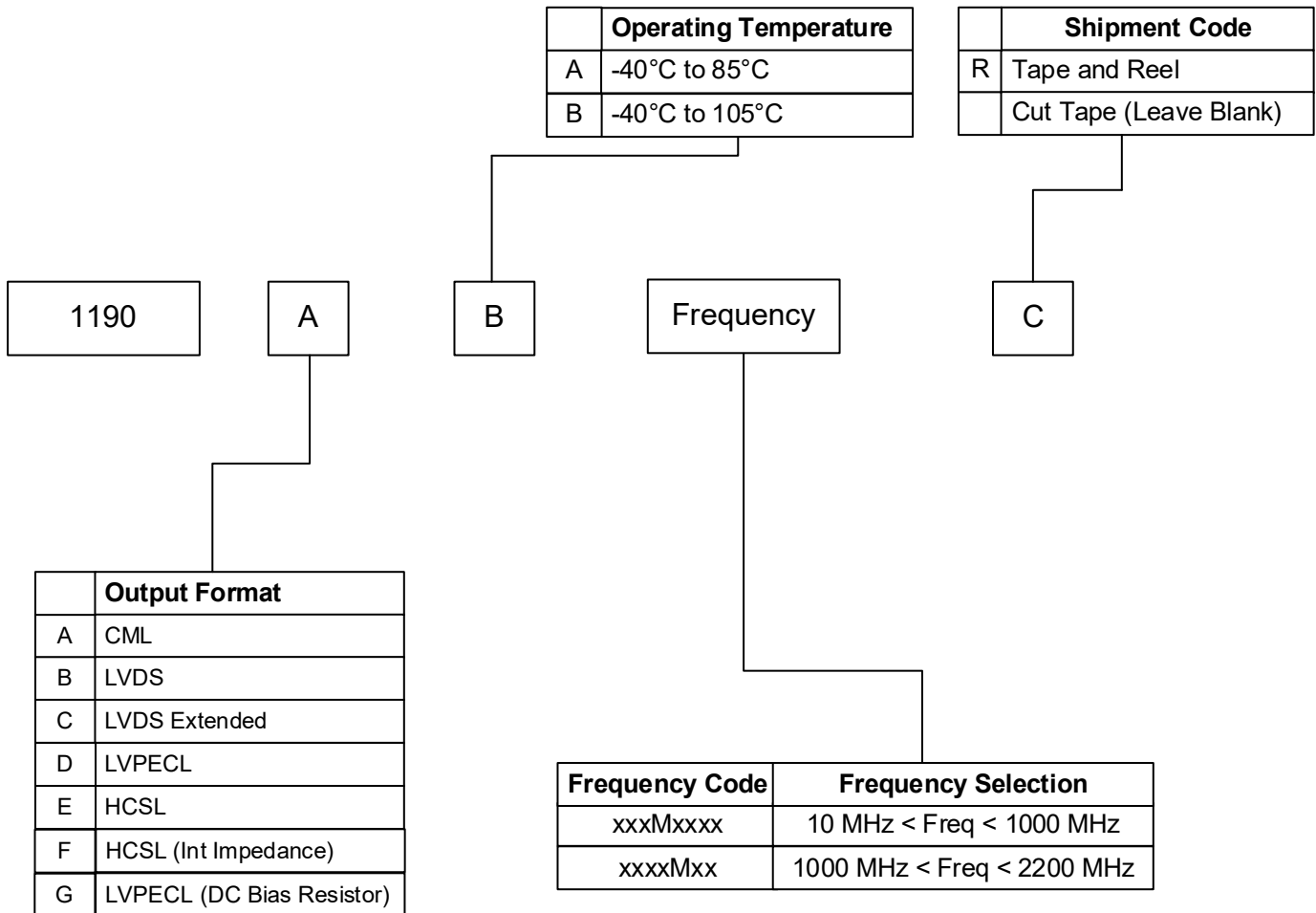


Figure 22. MS1190 Part Ordering Information

Table 11. Example of ordering part number

Base P/N	Output Format	Operating Temperature	Frequency Code	Shipment Type	Ordering part number
1190	HCSL	-40°C to 85°C	491.52 MHz	Tape and Reel	<b>1190FA491M5200R</b>
1190	LVPECL	-40°C to 85°C	1250 MHz	Tape and Reel	<b>1190DA1250M000R</b>

### Reflow Profile (IPC/JEDEC-STD-020)

Figure 23 shows the reflow profile for MS1190

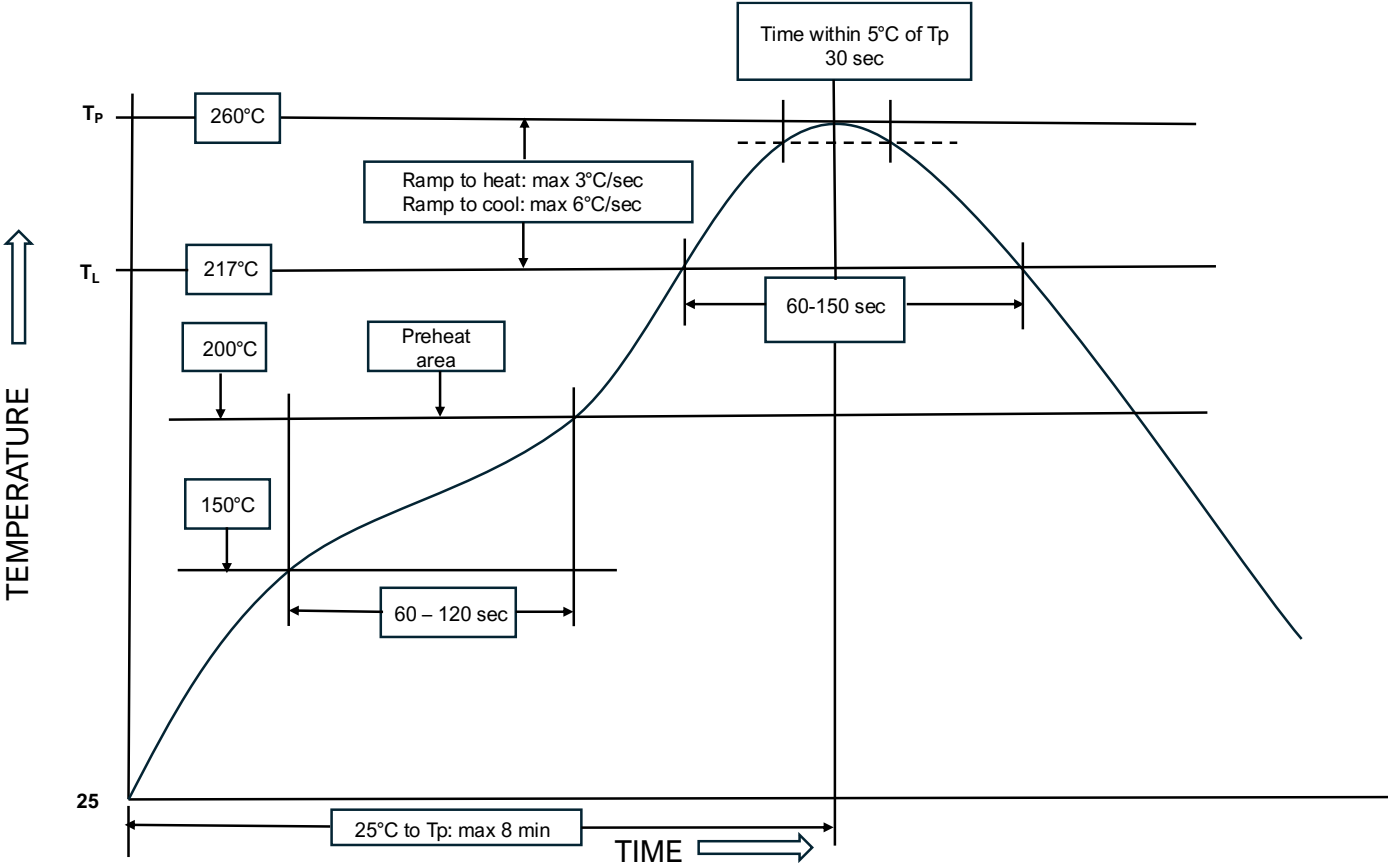


Figure 23. MS1190 Reflow Profile

## REVISION HISTORY

### Revision 1.1

April 20, 2026

- Added LVPECL Load Termination
- Updated ordering part number (include LVPECL Load Termination)

### Revision 1.0

December 5, 2025

- Initial Release

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