Preliminary Data Sheet

MS1130

Ultra-Low Jitter Crystal Oscillators (XO)

Features

- Available at any frequency from 10 MHz to 1000 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 43.1 fs at 156.25 MHz
  - 28.3 fs at 312.50 MHz
  - 31.8 fs at 491.52 MHz
  - 32.9 fs at 625 MHz
- Total stability of ±20 ppm
- CML/LVDS/LVDS-EXT/LVPECL/HCSL output formats
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Industry standard 2.5X2.0 mm 6-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- Network Equipment (Optical Modules, routers)
- 100G/200G/400G/800G OTN, Coherent optics
- Storage, switches, servers, NICs, accelerators
- Datacenter
- 3G to 24G SDI broadcast video
- 10G/40G/100G optical ethernet
- 56G/112G PAM4 Clocking
- Test and measurement equipment

General Description

The MS1130 is a crystal oscillator (XO) powered by our Virtual Crystal™ technology that enables very stable fully programmable multi-GHz clocks with extremely low phase noise.

Adaptive fully autonomous DSP algorithms running in the background continuously monitor and ensure robust and consistent performance over process, voltage and temperature variations.

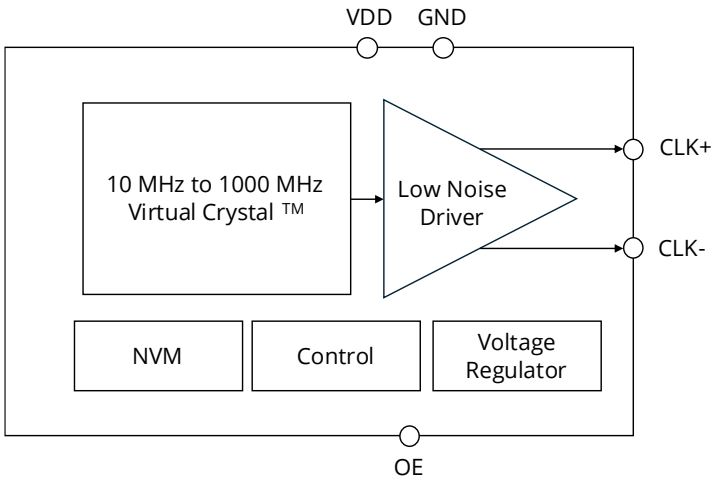
The devices are factory programmed to provide any frequency between 10 MHz and 1000 MHz with less than 1 ppb resolution.

The MS1130 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

Device Information

Part Number	Package	Description
MS1130	2.5x2.0 mm 6-pin LGA	XO

Figure 1. Functional Block Diagram



MS1130

Pin Assignment and Pin Description

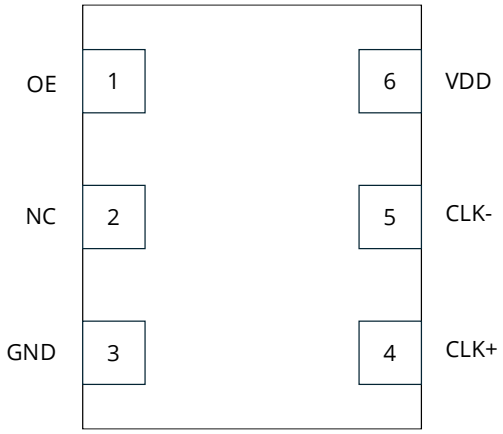


Figure 2. MS1130 Pin Assignments

Table 1. MS1130 Pin Descriptions

Pin No	Name	Description
1	OE	Output Enable
2	NC	No Connect
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply

Specifications

Table 2. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination. A 0.1uF and 10uf bypass capacitor should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Frequency Range	F_{CLK}	All Output Formats	10		1000	MHz
Frequency Stability						
Frequency Stability*	F_{STB}	-40°C to 105°C	-20		20	PPM
*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year, +25°C). Aging is estimated from environmental reliability tests;						
Clock Output Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz)	Φ_{JITTER}	Frequency=312.5 MHz		28.3		fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		1.71	1.8	1.89	V
Temperature Range	T_A	Industrial Temperature	-40		85	°C
		Extended Industrial Temperature	-40		105	°C

Current Consumption

Supply Current	I_{DD}	LVDS Output (Output Enabled)		80	100	mA
		All Other Outputs (Output Enabled)		90	110	mA
		Tristate Hi-Z (Output Disabled)		50	60	mA

Input Characteristics

Digital Input Levels(OE)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	us
	T_E	Output Enable Time			20	us
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

PSRR Characteristics

Power Supply-Induced Phase Noise	PSPN	Spurs induced by 50mV power supply ripples (312.5MHz)		-114		dBc
Power Supply-Jitter Sensitivity	PSJS			0.1		fs/mv

Note:

(1) Measured with 50 mVpp ripple from 50 KHz to 1 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		65	100	ps
LVDS Output (AC Mode)	Vpp	Differential Pk-Pk	0.5	0.7	0.9	V
LVDS Extended Output (AC Mode)	Vpp	Differential Pk-Pk	0.8	1.2	1.6	V
CML Output (AC Mode)	Vpp	Differential Pk-Pk	0.6	0.8	1	V
LVPECL Output (AC Mode)	Vpp	Differential Pk-Pk	1.2	1.4	1.6	V
HCSL Output	Vpp	Differential Pk-Pk	1.1	1.35	1.6	V
HCSL Output Voltage	V_{CM}	Common Mode Voltage	340	350	360	mV

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

Table 4. Environmental Compliance

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Moisture Sensitivity Level (MSL)	3
Note: For additional information not listed, please contact Mixed-Signal Devices.	

Table 5. ESD Levels

Description	Description	Specification	Level
HBM[1]	Human Body Model	JEDEC JS-001	2000V
CDM[2]	Charge Device Model	JEDEC JESD22-C101	500V

Notes:
1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155
2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157

Table 6. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
2.5mm x 2mm 6 pin LGA	Thermal Resistance, Junction to Ambient	$ø_{JA}$	90	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C

Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.

Table 7. Typical Output Phase Noise Characteristics
VDD= 1.8V, T_A = 25°C, Output Type = LVDS-EXT

Offset frequency	156.25 MHz	312.50 MHz	491.52 MHz	625 MHz	Unit
1 KHz	-102	-99	-95	-94	dBc/Hz
10 KHz	-133	-129	-125	-123	dBc/Hz
100 KHz	-157	-152	-146	-147	dBc/Hz
1 MHz	-165	-163	-156	-155	dBc/Hz
10 MHz	-165	-164	-157	-155	dBc/Hz
20 MHz	-165	-164	-159	-155	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	43.1	28.3	31.8	32.9	fs

Typical Output Measured Phase Noise Plots

This section shows MS1130 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = LVDS-EXT.

The plots were captured using an Agilent E5052B Signal Source Analyzer.

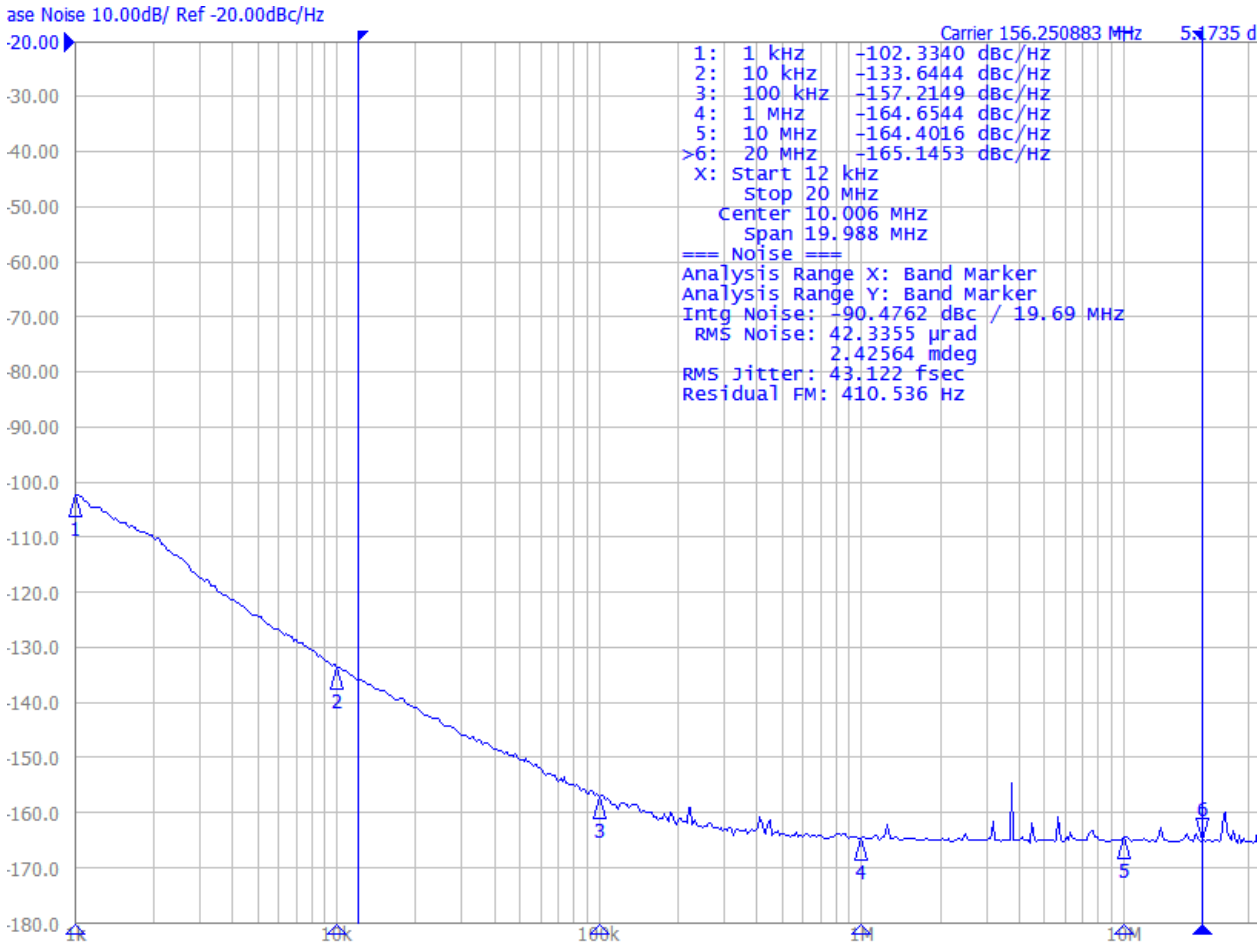


Figure 3. Carrier: 156.25 MHz

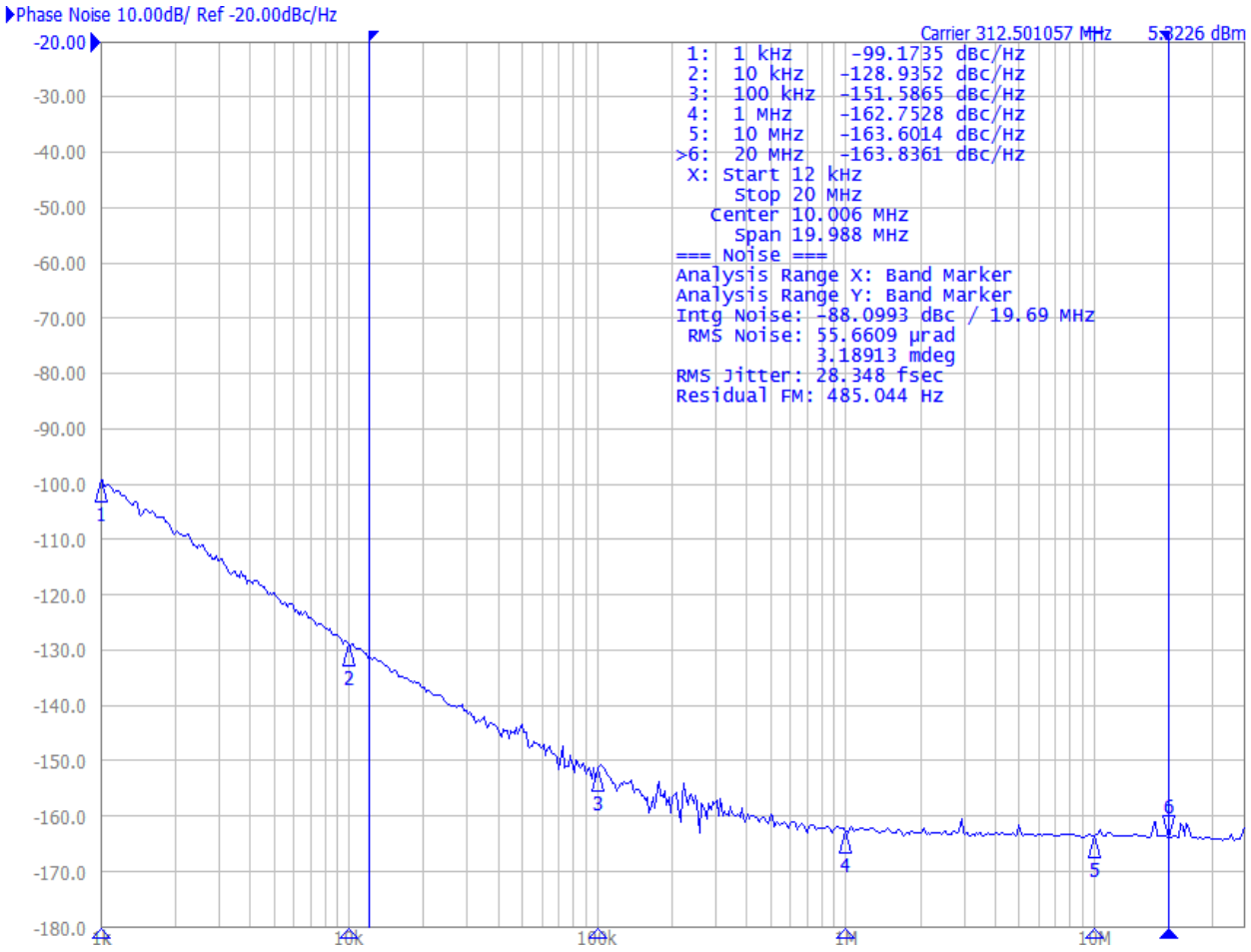


Figure 4. Carrier: 312.5 MHz

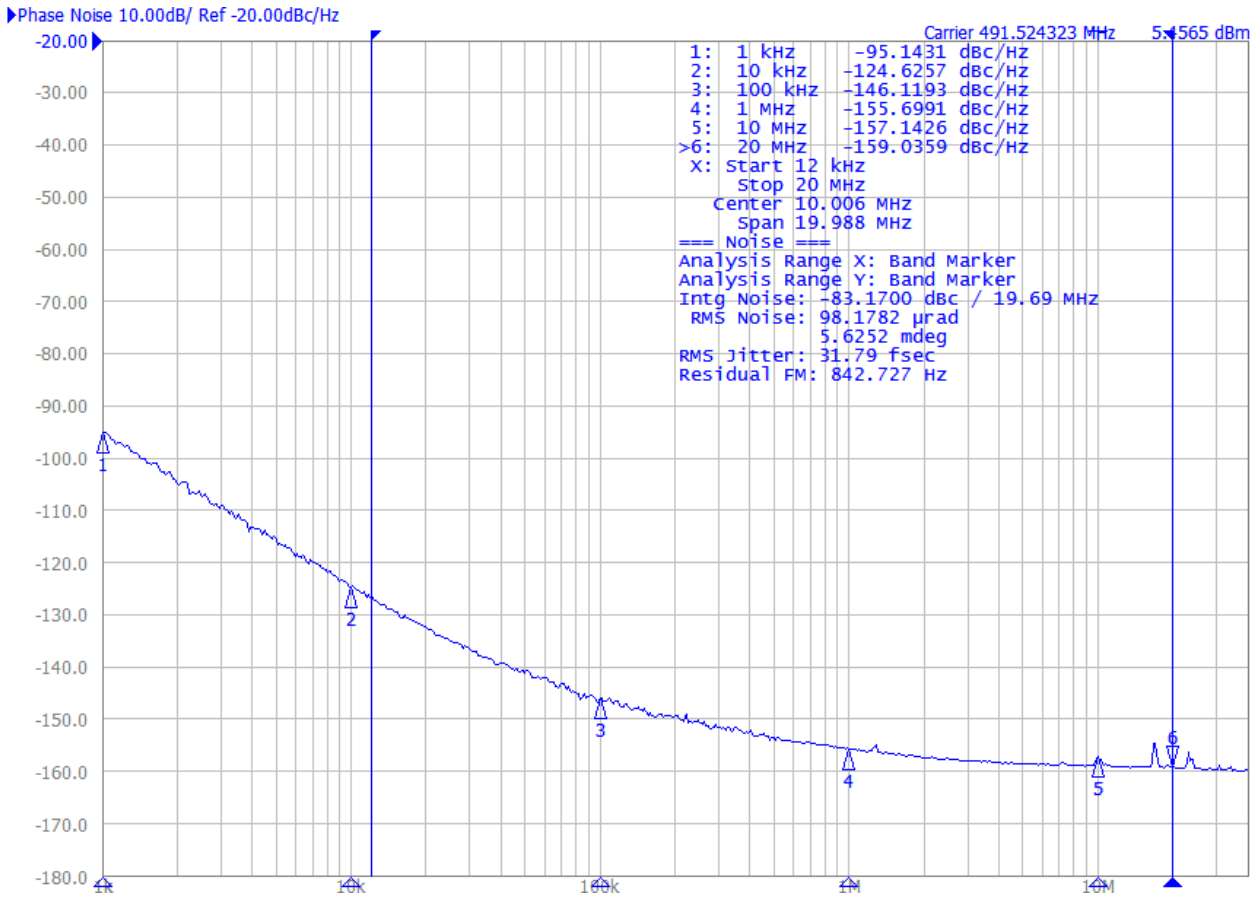


Figure 5. Carrier: 491.52 MHz

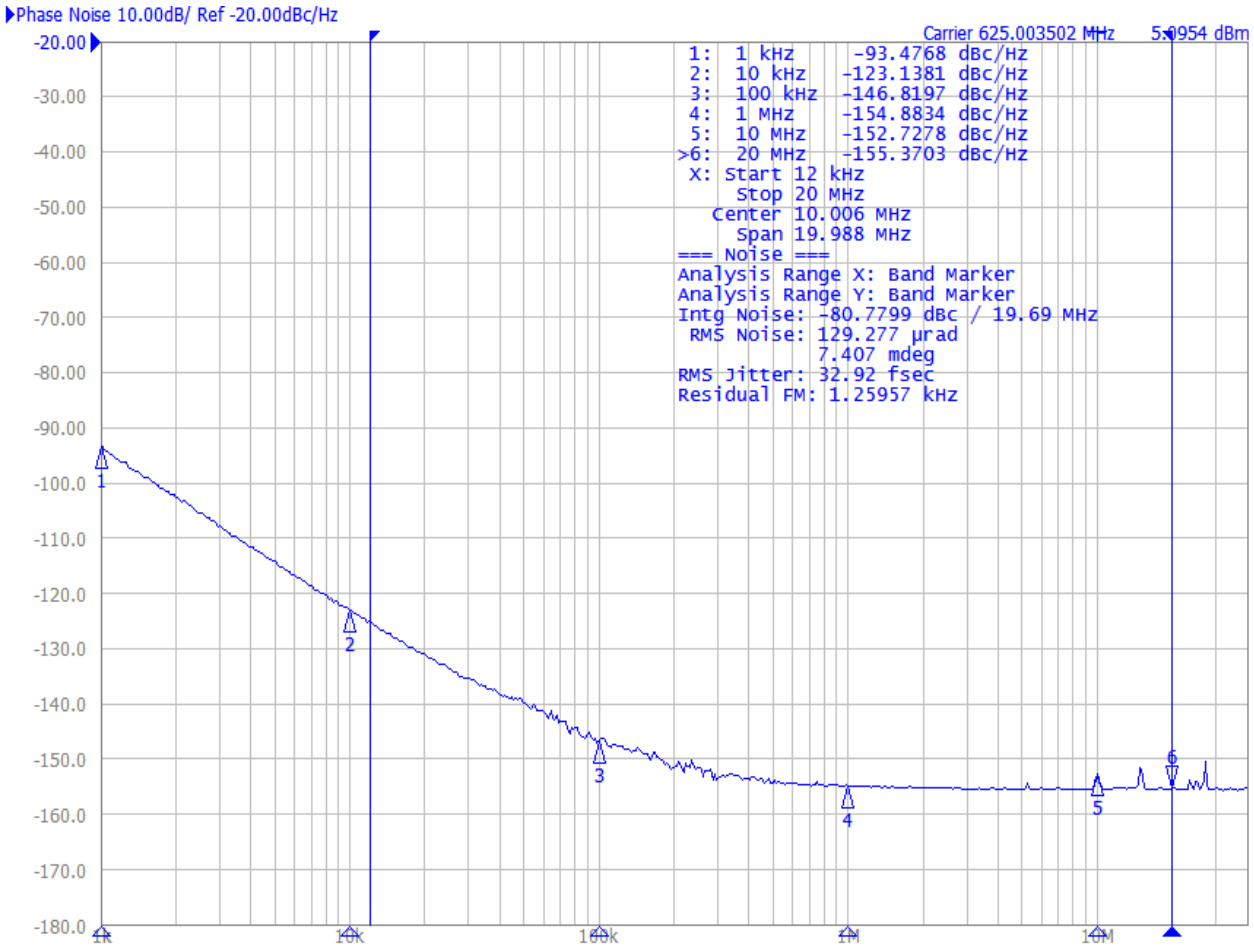


Figure 6. Carrier: 625 MHz

Output Terminations

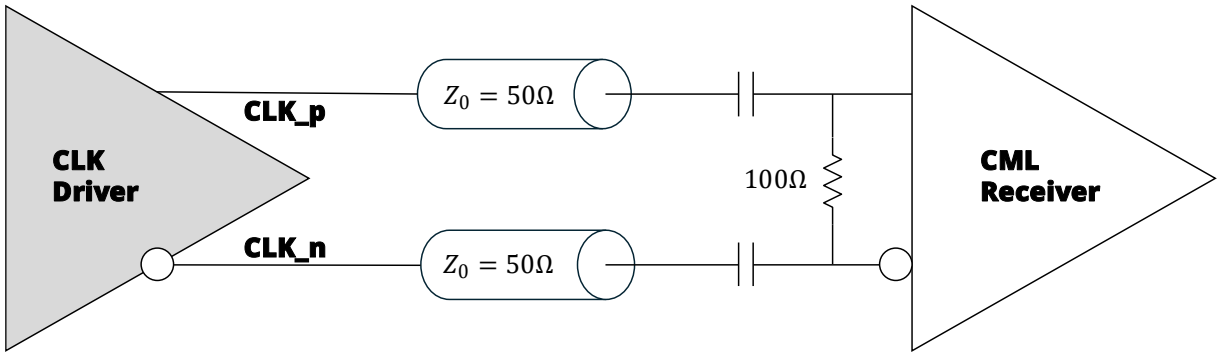


Figure 7. AC-Coupled CML

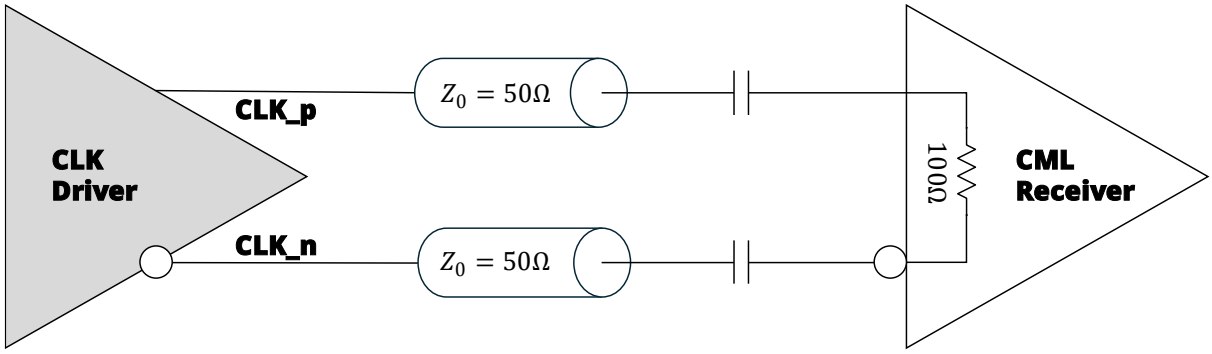


Figure 8. AC-Coupled CML (Receiver Termination)

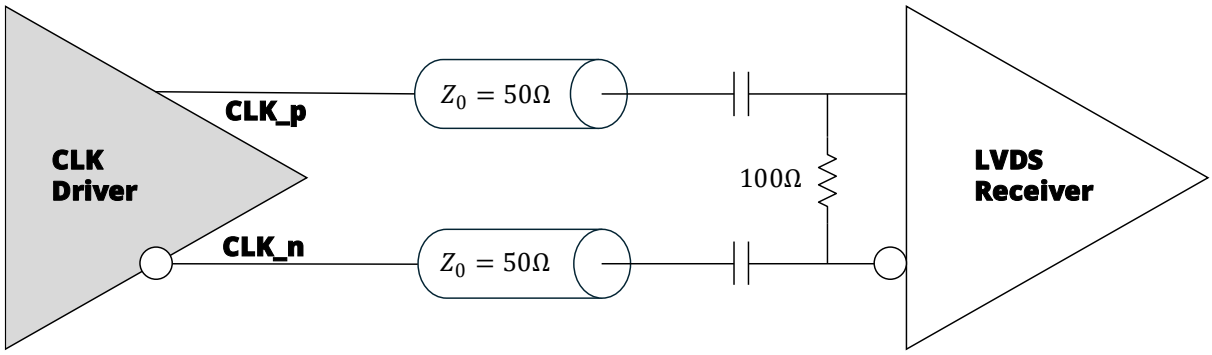


Figure 9. AC-Coupled LVDS

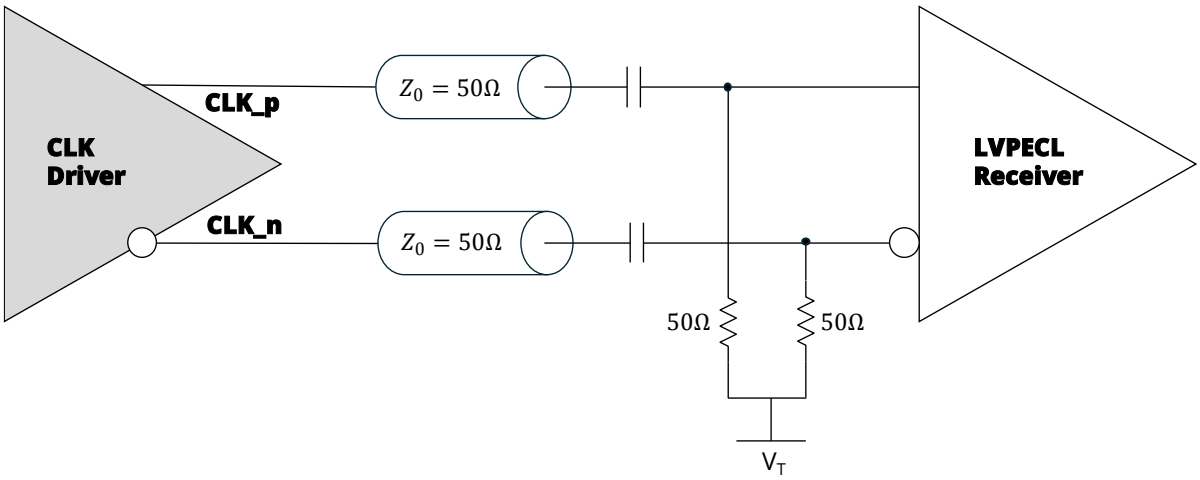


Figure 10. LVPECL (Receiver Termination)

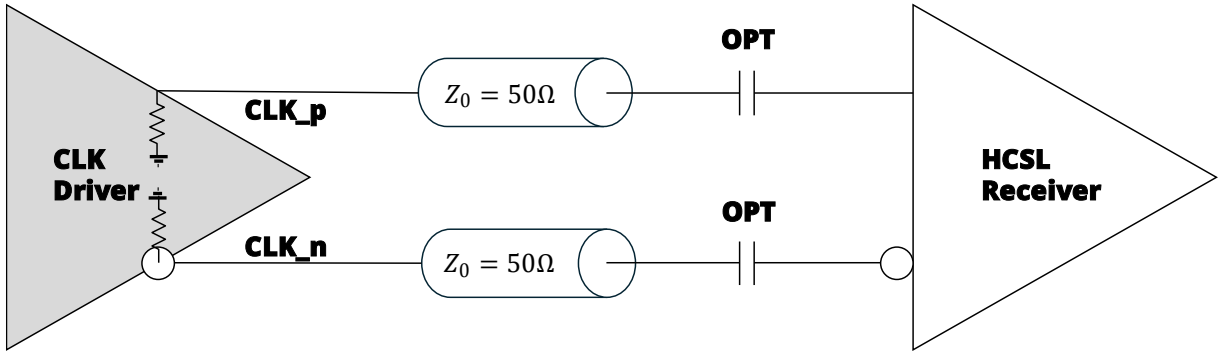


Figure 11. HCSL (Integrated Termination)

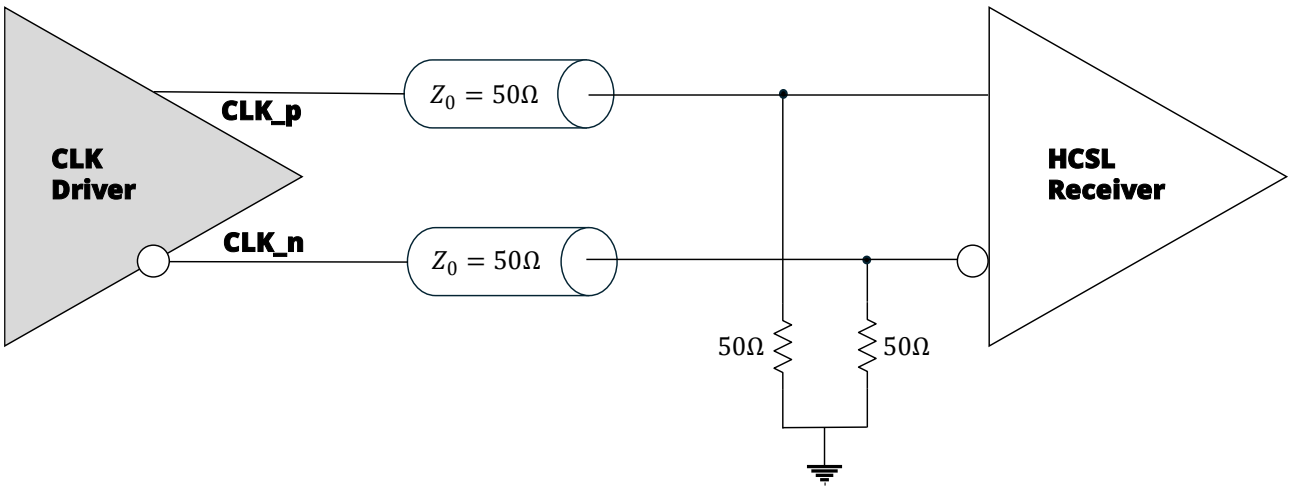


Figure 12. HCSL (Receiver Termination)

Output Timing

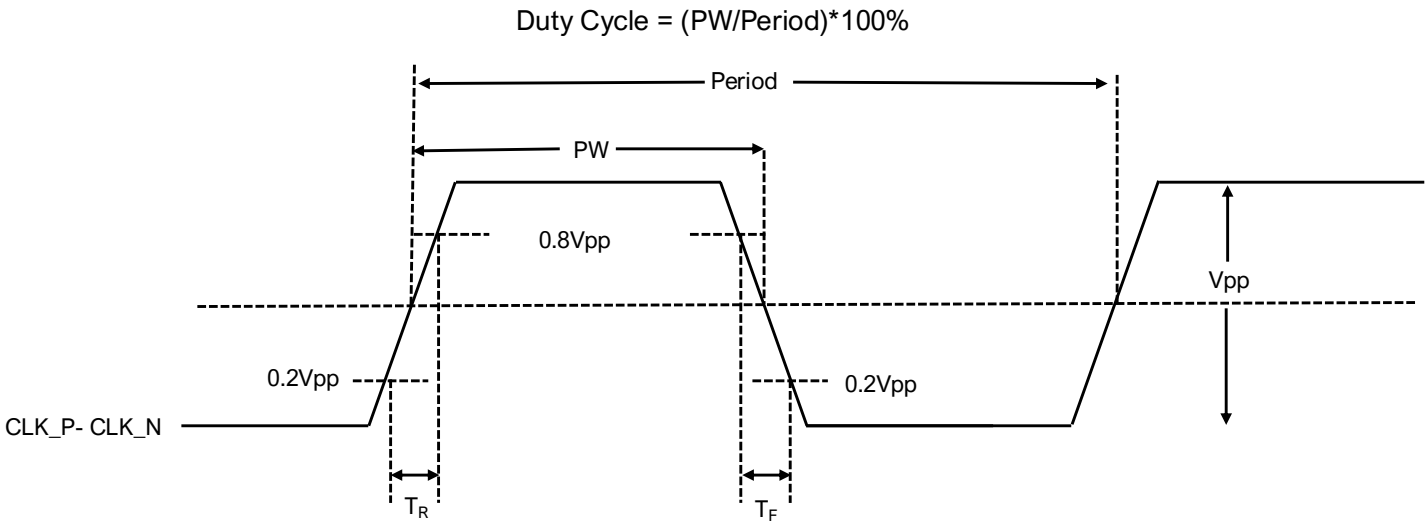


Figure 13. Output Timing across differential pair (CLK_P-CLK_N)

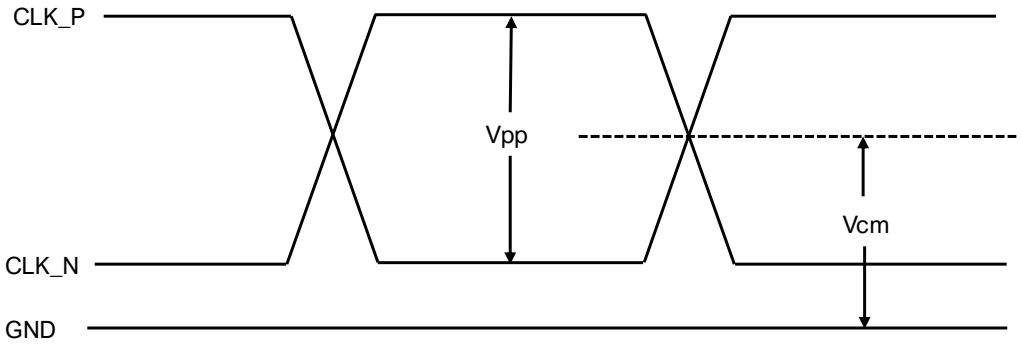


Figure 14. HCSL Output Level across differential pair (CLK_P-CLK_N)

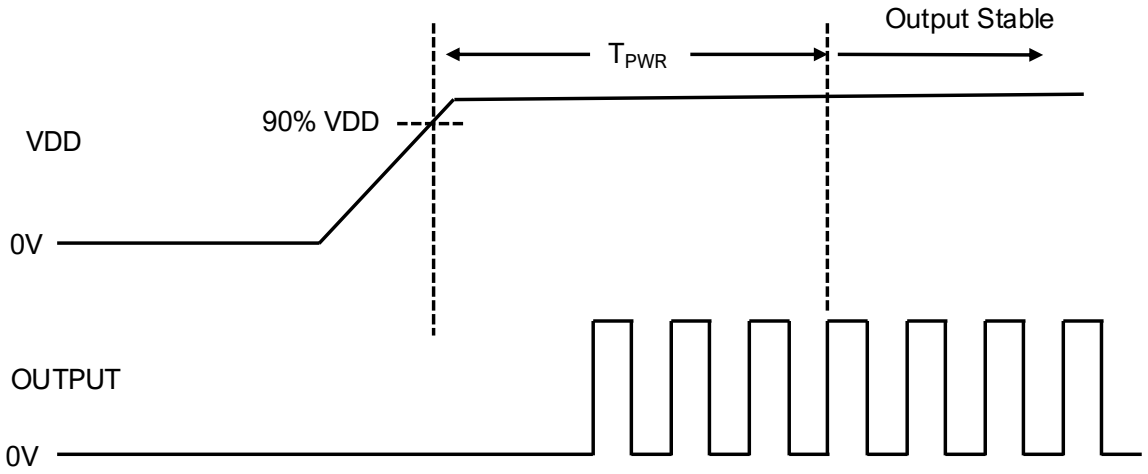


Figure 15. Powerup Timing

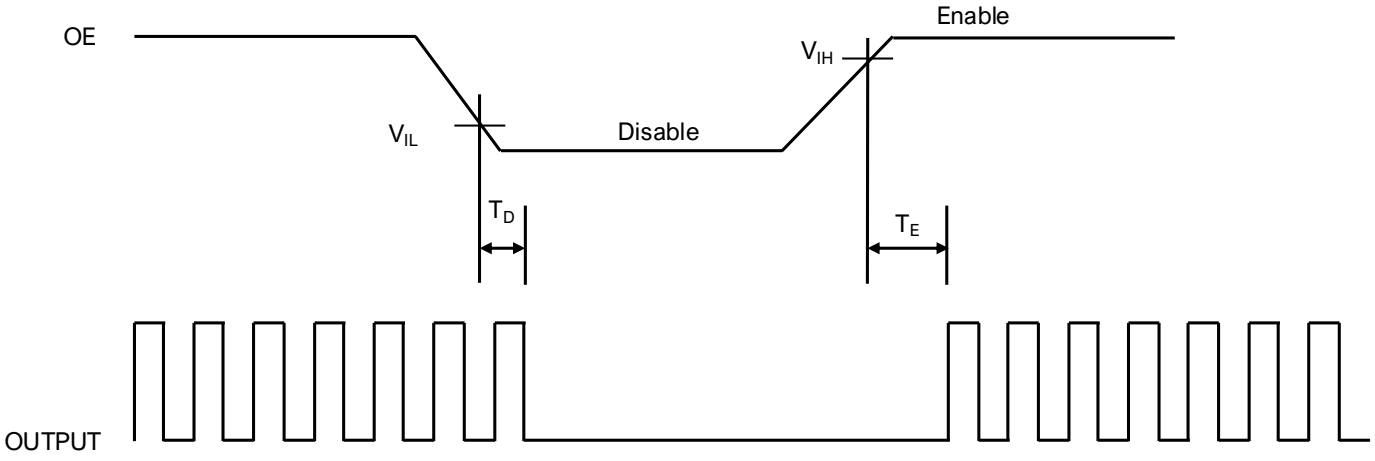


Figure 16. OE Enable/Disable Timing

Packaging Information

Figure 17 shows the MS1130 packaging drawing.

Figure 17. MS1130 Packaging Drawing (2.5X2.0 mm)

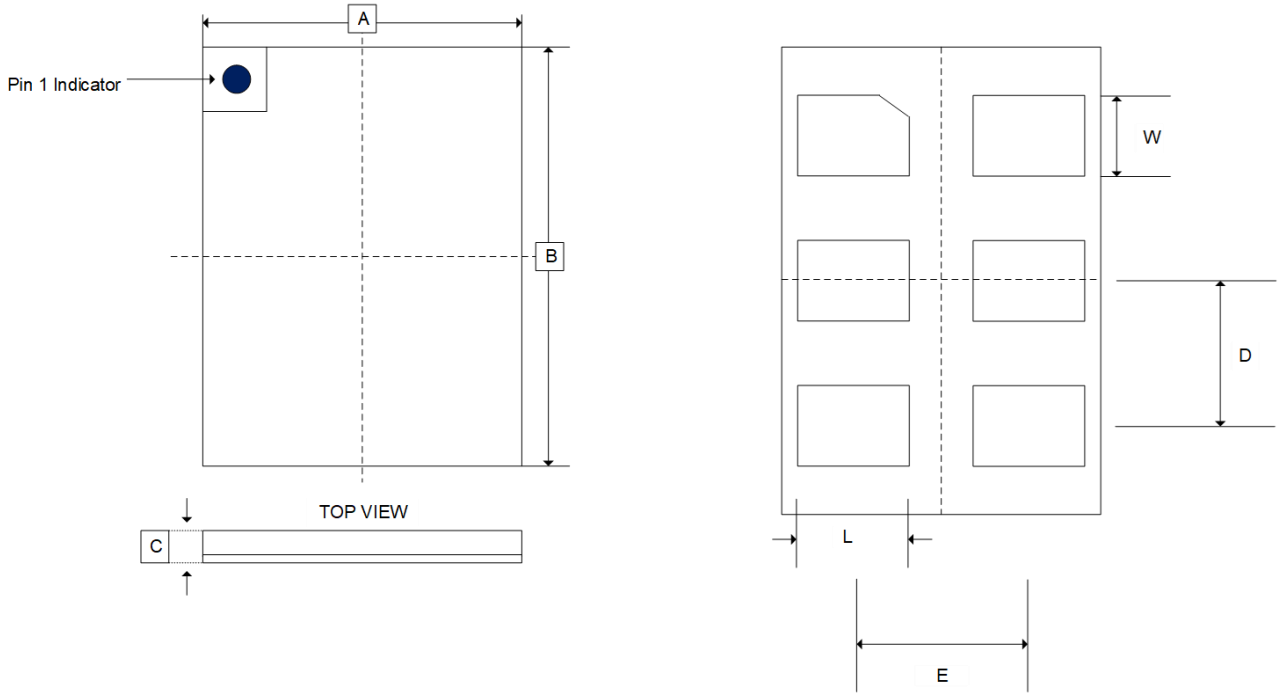


Table 8. MS1130 Packaging Dimensions

Dimensions	Min	Nom	Max
A		2.00 BSC	
B		2.50 BSC	
C	0.86	0.96	1.06
L	0.55	0.60	0.65
W	0.35	0.40	0.45
D		0.85 BSC	
E		1 BSC	
Package Edge Tolerance		0.1	
Mold Flatness		0.2	
Coplanarity		0.08	

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 18 shows the MS1130 PCB land pattern.

Note: All dimensions are in millimeters

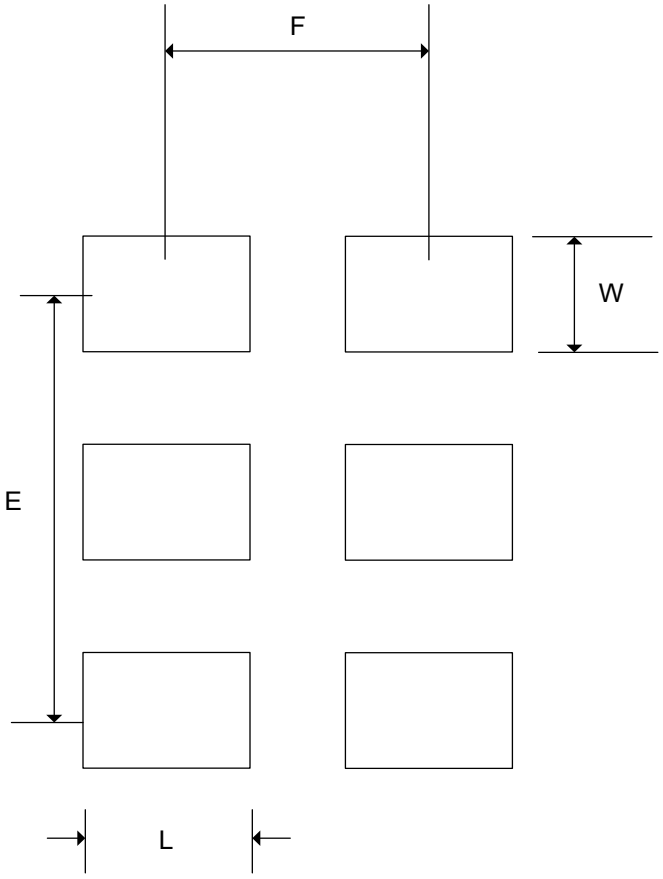


Figure 18. MS1130 Packaging Land Pattern Drawing (2.5X2.0 mm)

Table 9. MS1130 Packaging Land Pattern Dimensions

Dimensions	Length
L	0.75
W	0.55
E	1.7
F	1

Device Top Marking

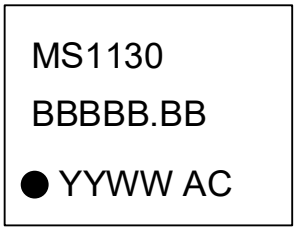


Figure 19. MS1130 Device Top Marking Showing Pin 1

Table 10. MS1130 Device Marking Legend

Line	Position	Description
1	1	Product Marking
2	1-5	Lot Number
	6-7	Wafer Number
3	Lot Trace Code	
	1	Pin 1 Orientation Mark (Dot)
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	7-8	Assembly Code

Part Ordering Information

Figure 20 shows a logic tree for ordering each of the available parts.

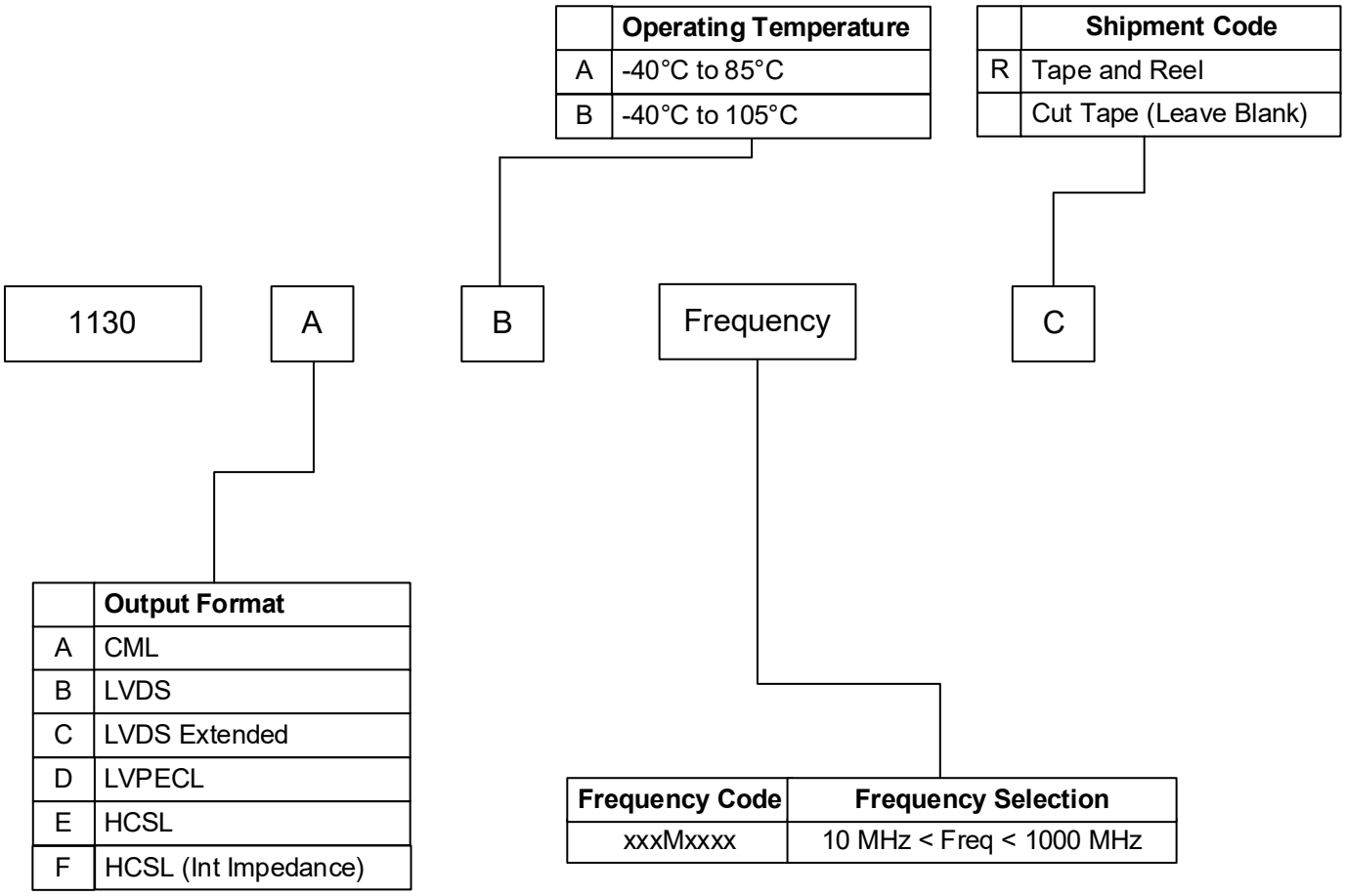


Figure 20. MS1130 Part Ordering Information

Table 11. Example of ordering part number

Base P/N	Output Format	Operating Temperature	Frequency Code	Shipment Type	**Ordering part number**
1130	LVDS	-40°C to 85°C	312.5 MHz	Tape and Reel	**1130BA312M5000R**
1130	LVPECL	-40°C to 105°C	625 MHz	Tape and Reel	**1130DB625M0000R**

Reflow Profile (IPC/JEDEC-STD-020)

Figure 21 shows the reflow profile for MS1130

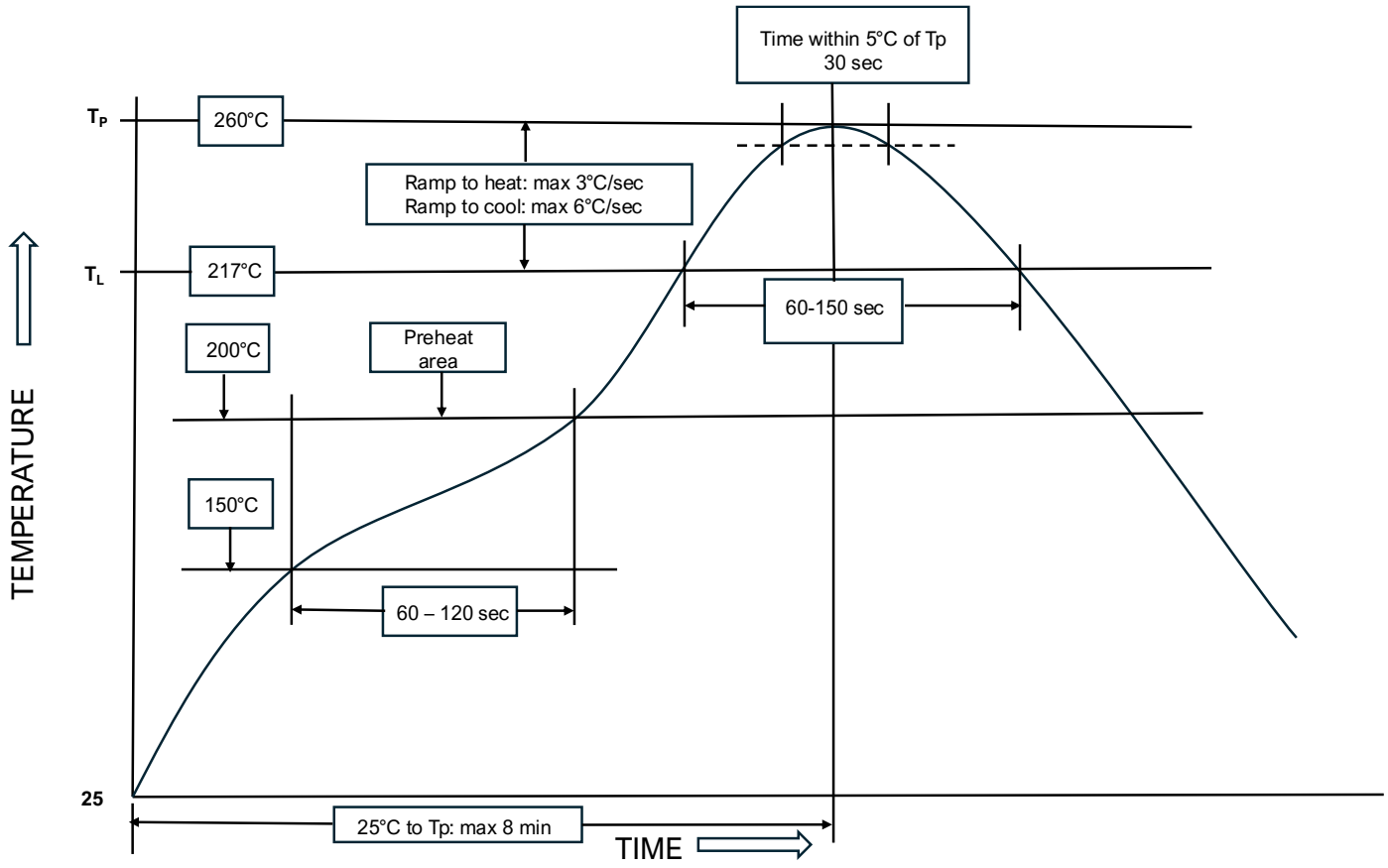


Figure 21. MS1130 Reflow Profile

REVISION HISTORY

Revision 1.2

October 17, 2025

- Updated Figure 13: Output Driver (HCSL); removed AC coupling
- Updated LVPECL Output Driver
- Updated limits for CML, HCSL
- Updated ordering part number

Revision 1.1

September 2, 2025

- Added Timing Diagram
- Updated Output Driver information (LVPECL, HCSL)
- Added Reflow Profile

Revision 1.0

December 20, 2024

- Initial Release

IMPORTANT NOTICE AND DISCLAIMER

MIXED-SIGNAL DEVICES INC. PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

Mailing Address: Mixed-Signal Devices Inc, 2 Venture, Suite 300, Irvine, California 92618, USA