

# **Ultra-High Performance Jitter Attenuator (JA)**

## **Features**

- Input frequency from 1 MHz to 750 MHz, gapped clock
- Output frequency from 10 MHz to 1000 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - o 32 fs at 312.50 MHz
  - o 34 fs at 491.52 MHz
- LVDS/CML/LVPECL/HCSL output formats
- Output Enable/Disable Feature
- < 10 ms start-up time
- 3.2X2.5 mm 8-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

## **Applications**

- Network Equipment
- Wireless Infrastructure, 5G
- High-end Video
- 40/100/400 GbE line cards
- Clock and data recovery
- Instrumentation and Medical Devices
- Test and Measurement

# Markette

## **General Description**

The MS1500 is a Jitter Attenuator powered by our Virtual Crystal<sup>™</sup> technology that enables ultra stable fully programmable multi-GHz clocks with extremely low phase noise.

Adaptive fully autonomous DSP algorithms running in the background continuously monitor and ensure robust and consistent performance over process, voltage, and temperature variations.

The product can take any input frequency from 1 MHz to 750 MHz and generate any output frequency from 10 MHz to 1000 MHz with <1ppb. The product is configured using factory programmed NVM.

The MS1500 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry

## **Device Information**

Part Number	Package	Description
MS1500	3.2X2.5 mm 8-pin LGA	Jitter Attenuator



Figure 1. Functional Block Diagram

# MS1500

## **Single Frequency Device**





## **Pin Assignment and Pin Description**





Table 1. MS1500 Pin Descriptions

Pin No	Name	Description
1	ICLK	Reference CLK input
2	OE	Output Enable
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply
7	NC	No Connect
8	NC	No Connect

# Specifications

#### Table 2. Electrical Specifications

Typical values are specified at  $T_A$ = 25°C,  $V_{DD}$ =1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination.

Parameter Symbol	Test Condition/Comment	Min	Тур	Мах	Unit
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#### **Frequency Range**

Input Frequency Range	Iclk		1	750	MHz
Input Voltage Swing	I <sub>SWG</sub>	AC-coupled	0.1	1.8	Vpp-SE
Output Frequency Range	Fclk	All Output Formats	10	1000	MHz

#### **Clock Output Jitter Characteristics**

RMS Phase Jitter	Φjitter	Frequency=312.5 MHz	32		<b>-</b>	
(12 KHz – 20 MHz)					FS	
Note:						
Phase jitter measured on Agilent 5052B Signal Source Analyzer						

#### **Operating Voltage/Temperature Range**

Supply Voltage	V <sub>DD</sub>		1.71	1.8	1.89	V
	_	Industrial Temperature	-40		85	°C
Temperature Range	TA	Extended Industrial Temperature	-40		105	°C

#### **Current Consumption**

		LVDS Output (Output Enabled)	80	100	mA
Supply Current	Supply Current	All Other Outputs (Output Enabled)	90	110	mA
		Tristate Hi-Z (Output Disabled)	50	60	mA

## Input Characteristics

Digital Input Levels	VIH		0.7XV <sub>DD</sub>		V
(OE)	VIL			0.3XV <sub>DD</sub>	V
Output Enable (OE)	T⊳	Output Disable Time		3	Us
	Τ <sub>Ε</sub>	Output Enable Time		20	Us
Powerup Time	Tpwr	Time from 0.9xVDD until output frequency (F <sub>CLK</sub> ) within spec		10	Ms

## **PSRR Characteristics**

PSRR	PSRRspur	Spurs induced by 50mV power supply ripples (All frequency, all output types)		-100		dBc
Note: (1) Measured max VDD Pin	mum spur le	evel with 50mVpp sinusoidal sig	gnal betwee	en 50 kHz a	and 1 MHz	applied on

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% VPP)	T <sub>R</sub> / T <sub>F</sub>	All Output Formats		65	100	Ps
LVDS Output (AC Mode)	Vo	Swing (Diff)	0.5	0.7	0.9	V
LVDS Extended Output (AC Mode)	Vo	Swing (Diff)	0.8	1.2	1.6	V
CML Output (AC Mode)	Vo	Swing (Diff)	0.7	0.85	1	V
LVPECL Output (AC Mode) Integrated Termination	Vo	Swing (Diff)	1.2	1.4	1.6	V
HCSL Output Integrated Termination	Vo	Swing (Diff)	1.2	1.4	1.6	V

Output Characteristics

## Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit			
1.8V Supply Voltage	-0.3	1.98	V			
Digital I/O	-0.3	1.98	V			
Maximum Operating Temperature		105	°C			
Storage Temperature	-55	150	°C			
Soldering Temperature		260	°C			
Junction Temperature		150	°C			
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the						

#### Table 4. Environmental Compliance

Parameter	Test Condition				
Mechanical Shock	MIL-STD-883, Method 2002				
Mechanical Vibration	MIL-STD-883, Method 2007				
Moisture Sensitivity Level (MSL)	3				
Note: For additional information not listed, please contact Mixed-Signal Devices.					

#### Table 5. ESD Levels

Description	Description	Specification	Level		
HBM <sup>1</sup>	Human Body Model	JEDEC JS-001	2000V		
CDM <sup>2</sup>	Charge Device Model	JEDEC JESD22-C101	500V		
Notes: 1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155 2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157					

#### Table 6. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
	Thermal Resistance, Junction to Ambient		80	°C/W
3.2mmX2.5mm	Thermal Resistance, Junction to Board	Ø <sub>JB</sub>	40	°C/W
8 pin LGA	Air Flow Condition		0	mps
	Maximum Junction Temperature	ТJ	125	°C
Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

## Table 7. Typical Output Phase Noise Characteristics

VDD= 1.8V, T<sub>A</sub> = 25°C, Output Type = CML

Offset frequency	156.25 MHz	312.50 MHz	491.52 MHz	625.00 MHz	Unit
1 KHz	-107	-101	-96	-94	dBc/Hz
10 KHz	-136	-130	-126	-124	dBc/Hz
100 KHz	-156	-152	-148	-145	dBc/Hz
1 MHz	-165	-161	-156	-153	dBc/Hz
10 MHz	-166	-162	-157	-154	dBc/Hz
20 MHz	-166	-162	-157	-154	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	39.8 fs	31.9 fs	34.3 fs	38.2 fs	fs

# **Typical Output Measured Phase Noise Plots**

This section shows four MS1500 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = CML.

The plots were captured using an Agilent 5052B Signal Source Analyzer.



Figure 4. Carrier: 156.25 MHz



Figure 5. Carrier: 312.5 MHz



#### Phase Noise 10.00dB/ Ref -20.00dBc/Hz

Figure 6. Carrier: 491.52 MHz



Figure 7. Carrier: 625 MHz

# Overview

The MS1500 is a single channel high-performance Jitter Attenuator that offers exceptional capabilities in the generation of an ultra-low phase noise clock, making it an ideal solution for next-generation communication systems and base stations. This device can produce one differential output clock synchronized to the reference clock input with input frequency ranging from 1MHz to 750MHz single-ended, and gapped clock support. The MS1500 boasts an output frequency range of 10MHz to 1GHz and a remarkably low RMS jitter of 40fs (12KHz to 20MHz), making it one of the most reliable and precise devices available.

The device's programmability is configured by on-chip non-volatile memory (NVM). This attribute permits the MS1500 to provide great flexibility and ease of use in a broad range of applications, including telecommunications, networking, and test and measurement equipment.

# **Functional Description**

The MS1500 is an all-digital Phase-Locked Loop (PLL) that incorporates a range of features to enable jitter attenuation and programmable multiplication of input frequency. It receives one reference clock input and generates any multiplication of the input clock using fractional multipliers and high-speed output divider. The device can output various formats, such as LVDS, CML, LVPECL, and HCSL.

1. Frequency Configuration

The frequency configuration of the PLL is programmable through the serial interface and can also be stored in nonvolatile memory. The combination of fractional frequency multiplication (M/N) and integer output division (Rn) allows the generation of any output frequency on any of the outputs. Fractional multiplication ratio and output divider ratio values can be easily calculated by the EZ-cleaner GUI utility.

2. PLL loop bandwidth

The PLL loop bandwidth determines the amount of input clock jitter attenuation. Register configurable PLL loop bandwidth settings in the range of 0.01 Hz to 4 kHz are available for selection in the EZ-cleaner GUI utility. Since the loop bandwidth is controlled digitally, the PLL will always remain stable with less than 0.1 dB of peaking regardless of the loop bandwidth selection.

# **Operation Modes**

## Free Running Mode (Default Mode)

After initialization, MS1500 will enter free running mode. In this mode, the device generates an output clock using multiplication factor stored in the on-chip NVM. The frequency accuracy of the generated output clock tracks the frequency accuracy of the input reference. For example, if the input frequency is 156.25 MHz (+/- 10ppm) and the stored multiplication factor is 33/32, the output frequency would be 161.1328125 MHz (+/- 10ppm).

## Lock Acquisition Mode.

Upon completion of the configuration process, the MS1500 will transition into the lock acquisition mode. This mode comprises two stages: fast acquisition and narrow acquisition. In the first stage, the loop bandwidth is widened to facilitate a speedy initial acquisition process. Following this, the bandwidth is narrowed as the device completes the lock.

# Output

MS1500 supports CML, LVDS, LVPECL, and HCSL output formats. The output enable, OE, is active HI. When OE is LOW, MS1500 output will be High Z but the loop will stay locked.

# **Output Terminations**



Figure 8. AC-Coupled CML



Figure 9. AC-Coupled CML (Receiver Termination)







Figure 11. AC-Coupled LVPECL (Integrated Termination)



Figure 12. HCSL (Integrated Termination)

# **Packaging Information**

Figure 13 shows the MS1500 packaging drawing.



Figure 13. MS1500 Packaging Drawing (3.2mm x 2.5 mm)

Table	8. N	<b>NS1</b>	500	Packa	aging	Dime	ensions
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Dimensions	Min	Nom	Мах
А	2.5 BSC		
В		3.2 BSC	
С	0.806	0.946	1.1
W	0.55	0.6	0.65
L	0.5	0.55	0.6
W1	0.35	0.4	0.45
L1	0.35	0.4	0.45
е	1.1 BSC		
D1	2.2 BSC		
Package Edge Tolerance	0.1		
Mold Flatness	0.1		
Coplanarity	0.08		

# **Packaging Land Pattern**

Figure 14 shows the MS1500 PCB land pattern.



Figure 14. MS1500 Packaging Land Pattern Drawing (3.2mm x 2.5mm)

Dimensions	In mm
L	0.7
W	0.7
L1	0.5
W1	0.55
E	1.1
F	2.6
G	1.76

Table 9. MS1500 Packaging Land Pattern Dimensions

# **Device Top Marking**



## Figure 15. MS1500 Device Top Marking Showing Pin 1

Line	Position	Description		
1	1	Part Number		
2	1-5	Wafer Lot Number		
6-7		Wafer #		
		Lot Traceability		
	1	Pin 1 Orientation Mark (Dot),		
3	2-3	Year (last two digits of the year)		
	4-5	Calendar Work Week Number (1-53)		
6-7 Assembly Code		Assembly Code		

#### Table 10. MS1500 Device Marking Legend

# **Part Ordering Information**

Figure 16 shows a logic tree for ordering each of the three available parts.



Figure 16. MS1500 Part Ordering Information

Code (xxx)	Frequency (MHz)	Code (yyy)	Frequency (MHz)
001	1	050	50
100	100	100	100
106	106.25	106	106.25
122	122.88	122	122.88
153	153.6	153	153.6
156	156.25	156	156.25
212	212.5	212	212.5
245	245.76	245	245.76
250	250	250	250
307	307.2	307	307.2
312	312.5	312	312.5
322	322.2656525	322	322.2656525
491	491.52	491	491.52
500	500	500	500
614	614.4	614	614.4
625	625	625	625
644	644.53125	644	644.53125
750	750	983	983.05

Input/Output Frequency codes for ordering

Please contact Mixed-Signal Devices for additional frequency codes

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