Preliminary Data Sheet

MS1220

Ultra-Low Jitter Crystal Oscillators (VCXO)

Features

- Available at any frequency from 10 MHz to 1000 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 32 fs at 312.50 MHz
  - 34 fs at 491.52 MHz
- Total stability of ±5 ppm
- Programmable tuning slope (Kvco) up to 300 ppm/V
- CML/LVDS/LVPECL/HCSL output formats
- Simplified BoM with no external loop filters
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Industry standard 3.2X2.5 mm 8-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- SONET/SDH
- 10 GbE LAN/WAN
- Wireless Infrastructure
- Synchronous Ethernet
- Optical modules
- Clock and data recovery
- Clock Generation and Frequency Translation
- High-performance replacement for SAW

General Description

The MS1220 is a voltage-controlled crystal oscillator (VCXO) powered by our Virtual Crystal™ technology that enables ultra stable fully programmable multi-GHz clocks with extremely low phase noise.

Adaptive fully autonomous DSP algorithms running in the background continuously monitor and ensure robust and consistent performance over process, voltage, and temperature variations.

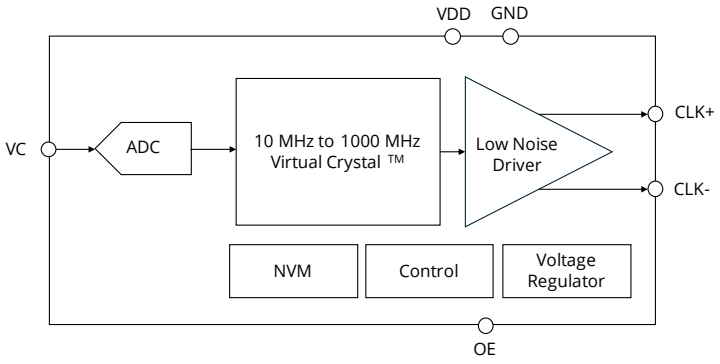
The devices are factory programmed to provide any frequency between 10 MHz and 1000 MHz with less than 1 ppb resolution.

The MS1220 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

Device Information

Part Number	Package	Description
MS1220	3.2X2.5 mm 8-pin LGA	Single frequency

Figure 1. Functional Block Diagram



MS1220

Single Frequency Device

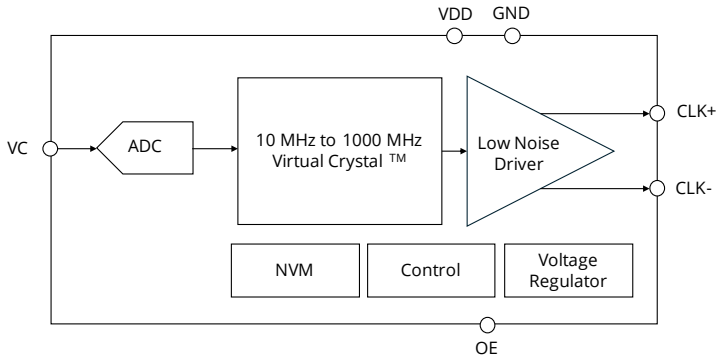


Figure 2. MS1220 Functional Block Diagram

Pin Assignment and Pin Description

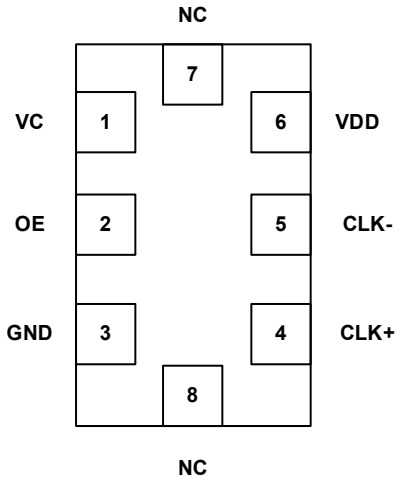


Figure 3. MS1220 Pin Assignments

Table 1. MS1220 Pin Descriptions

Pin No	Name	Description
1	VC	Control Voltage
2	OE	Output Enable
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply
7	NC	No Connect
8	NC	No Connect

Specifications

Table 2. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination. A 0.1uF and 10uf bypass capacitor should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit
Frequency Range						
Frequency Range	F_{CLK}	All Output Formats	10		1000	MHz
Frequency Stability						
Frequency Stability*	F_{STB}	-40°C to 85°C	-5		5	PPM
Frequency Stability*	F_{STB}	-40°C to 105°C	-20		20	PPM
*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year, +25°C). Aging is estimated from environmental reliability tests;						
Clock Output Jitter Characteristics						
RMS Phase Jitter (12 KHz – 20 MHz)	Φ_{JITTER}	Frequency=312.5 MHz		32		fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						
Operating Voltage/Temperature Range						
Supply Voltage	V_{DD}		1.71	1.8	1.89	V
Temperature Range	T_A	Industrial Temperature	-40		85	°C
		Extended Industrial Temperature	-40		105	°C
Current Consumption						

Supply Current	I_{DD}	LVDS Output (Output Enabled)		80	100	mA
		All Other Outputs (Output Enabled)		90	110	mA
		Tristate Hi-Z (Output Disabled)		50	60	mA

Input Characteristics

Digital Input Levels (OE)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	us
	T_E	Output Enable Time			20	us
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

PSRR Characteristics

PSRR	$PSRR_{SPUR}$	Spurs induced by 50mV power supply ripples (All frequency, all output types)		-100		dBc

Note:

(1) Measured maximum spur level with 50mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		65	100	ps
LVDS Output (AC Mode)	V_O	Swing (Diff)	0.5	0.7	0.9	V
LVDS Extended Output (AC Mode)	V_O	Swing (Diff)	0.8	1.2	1.6	V
CML Output (AC Mode)	V_O	Swing (Diff)	0.7	0.85	1	V
LVPECL Output (AC Mode) Integrated Termination	V_O	Swing (Diff)	1.2	1.4	1.6	V
HCSL Output Integrated Termination	V_O	Swing (Diff)	1.2	1.4	1.6	V

Vc Control Voltage Input

Parameter	Symbol	Test Condition/Comment	Min		Typ	Max	Unit
Control Voltage Tuning Slope1	Kvco	0.1V to 0.9V			50		ppm/V
					100		
					150		
					200		
					250		
					300		
Control Voltage Linearity	Lvc	Best Straight Line Fit	-1.5		±0.5	+1.5	%
		KVCO Variation	-10		±5	+10	%
Modulation Bandwidth	BW				10		kHz
Vc Input Impedance	Zvc		500				kΩ
Nominal Control Voltage	Vcnom	@fo			0.5		V
Control Voltage Tuning Range	Vc		0.1			0.9	V

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C

Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.

Table 4. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
3.2mmX2.5mm 8 pin LGA	Thermal Resistance, Junction to Ambient	$ø_{JA}$	80	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C

Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.

Table 5. Environmental Compliance

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Moisture Sensitivity Level (MSL)	3
Note: For additional information not listed, please contact Mixed-Signal Devices.	

Table 6. ESD Levels

Description	Description	Specification	Level
HBM[1]	Human Body Model	JEDEC JS-001	2000V
CDM[2]	Charge Device Model	JEDEC JESD22-C101	500V

Notes:
1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155
2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157

Table 7. Typical Output Phase Noise Characteristics
VDD= 1.8V, T_A = 25°C, Output Type = CML

Offset frequency	156.25 MHz	312.50 MHz	491.52 MHz	625.00 MHz	Unit
1 KHz	-107	-101	-96	-94	dBc/Hz
10 KHz	-136	-130	-126	-124	dBc/Hz
100 KHz	-156	-152	-148	-145	dBc/Hz
1 MHz	-165	-161	-156	-153	dBc/Hz
10 MHz	-166	-162	-157	-154	dBc/Hz
20 MHz	-166	-162	-157	-154	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	39.8 fs	31.9 fs	34.3 fs	38.2 fs	fs

Typical Output Measured Phase Noise Plots

This section shows three MS1220 performance plots.

Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = CML.

The plots were captured using an Agilent 5052B Signal Source Analyzer.

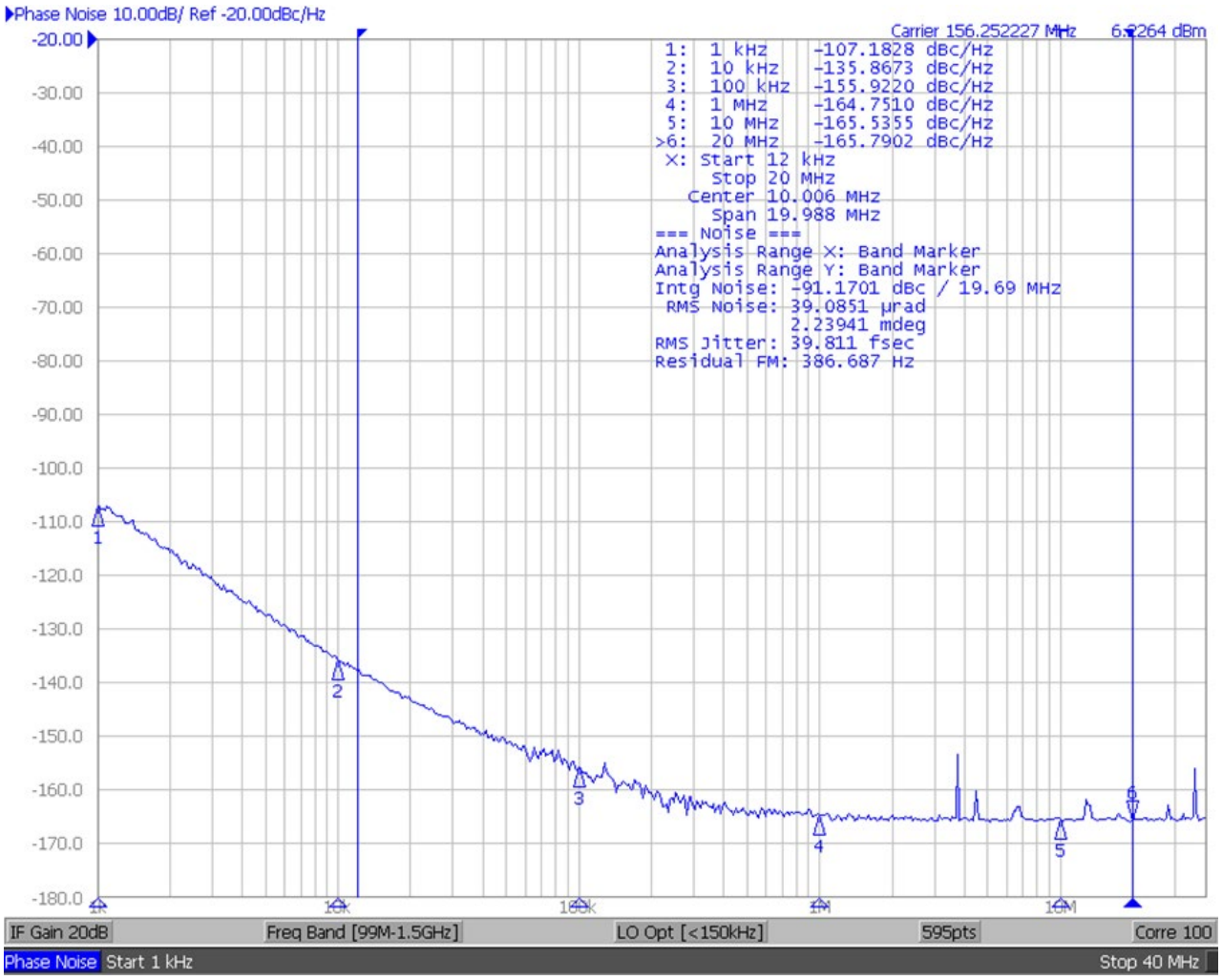


Figure 4. Carrier: 156.25 MHz

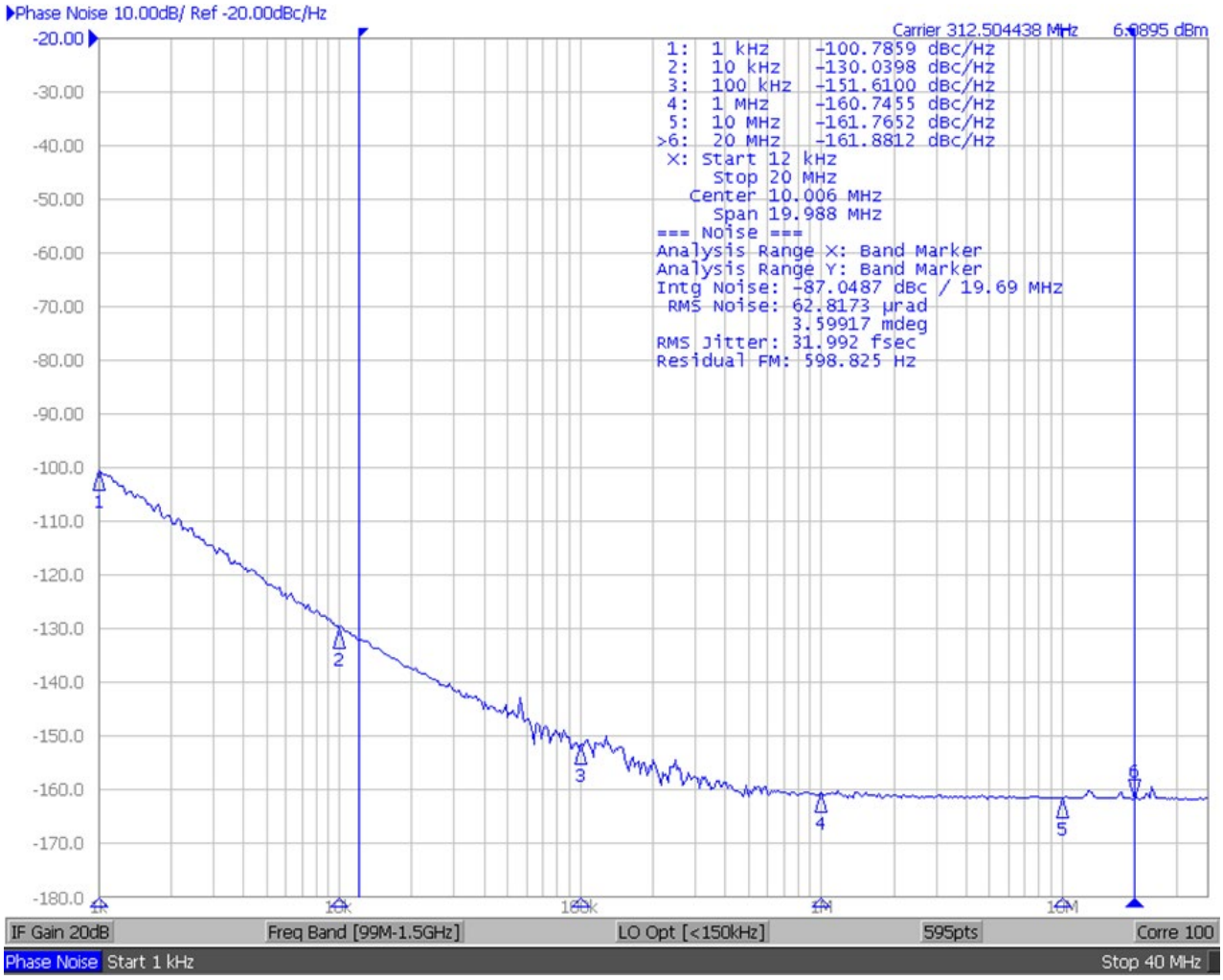


Figure 5. Carrier: 312.5 MHz

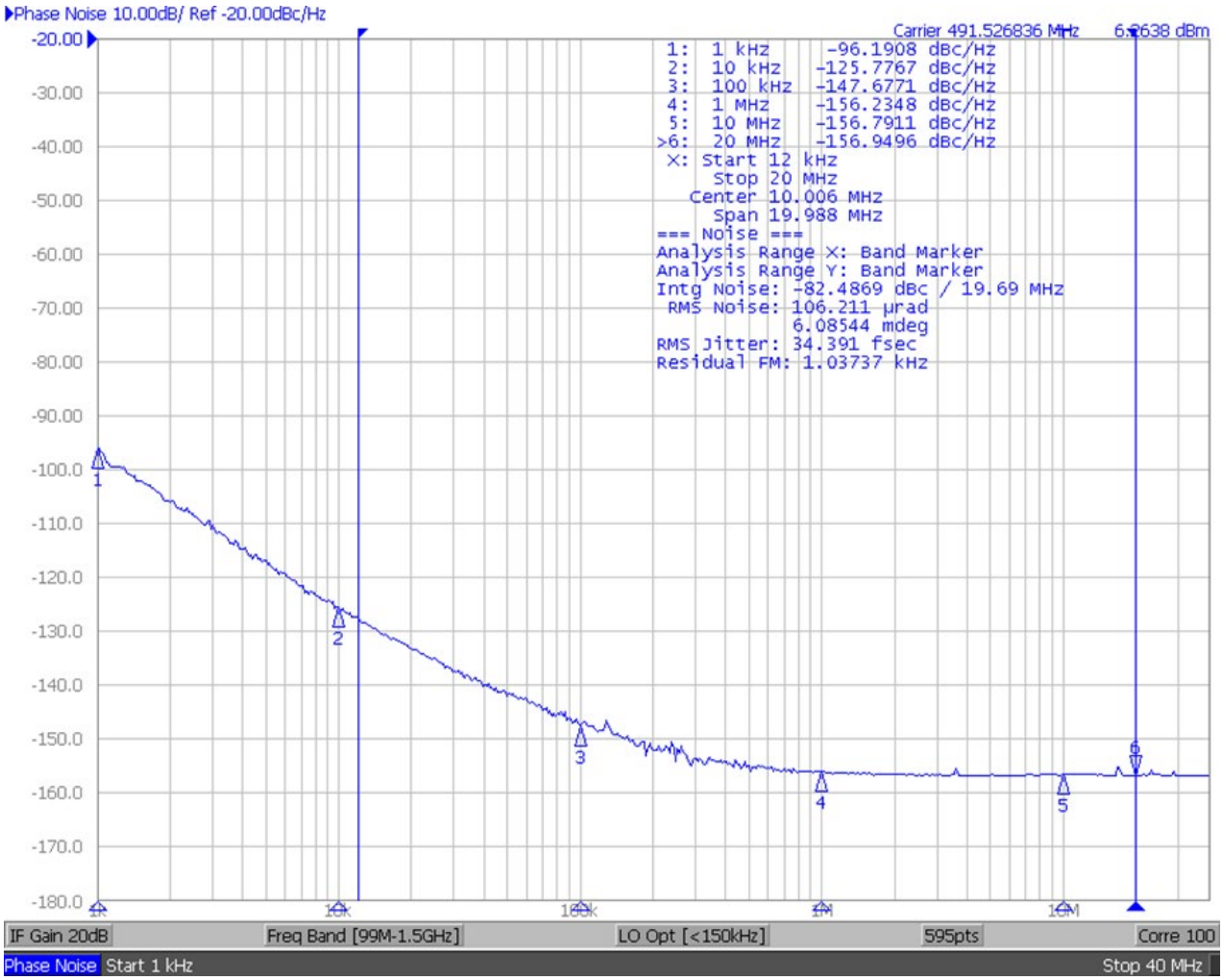


Figure 6. Carrier: 491.52 MHz

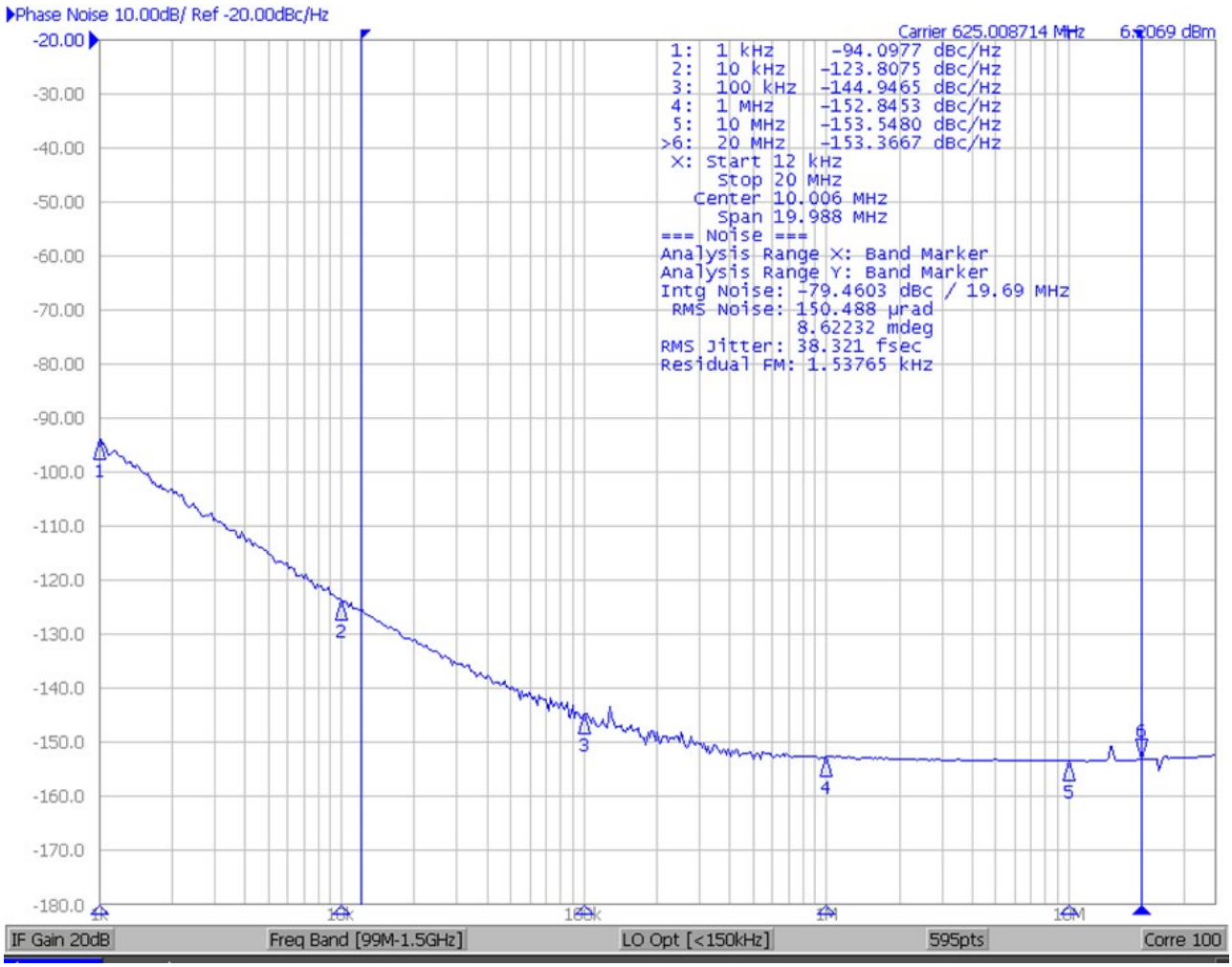


Figure 7. Carrier: 625 MHz

Output Terminations

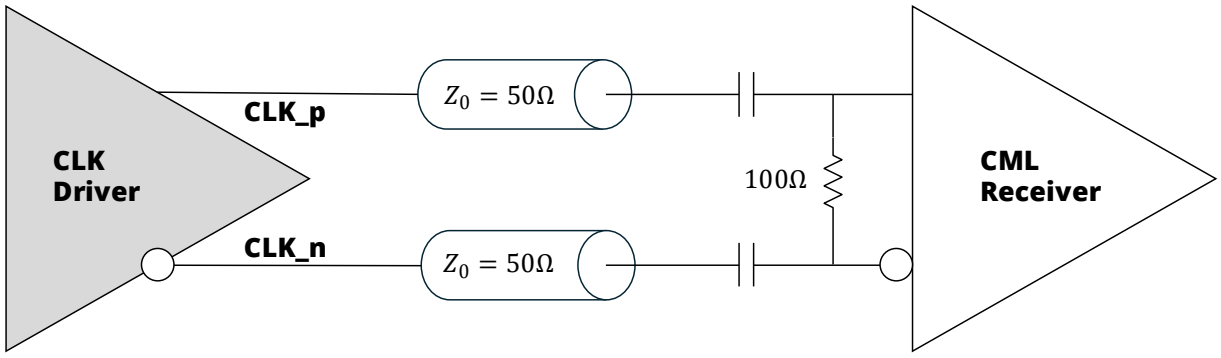


Figure 8. AC-Coupled CML

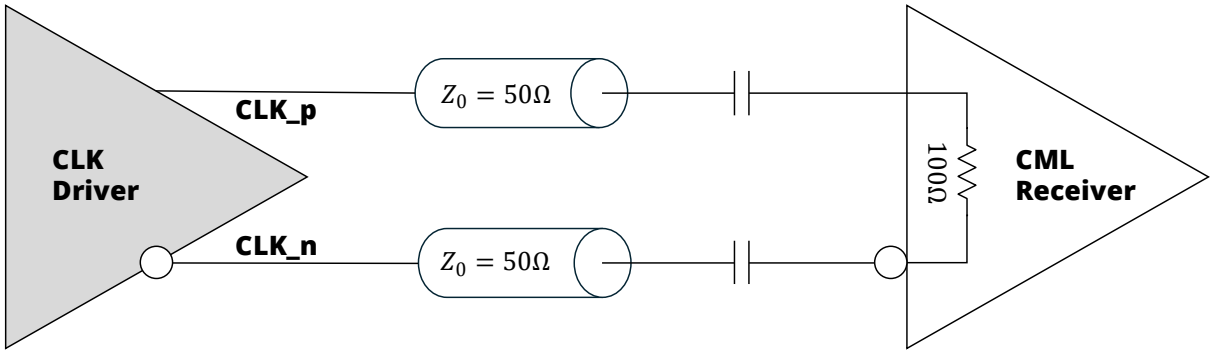


Figure 9. AC-Coupled CML (Receiver Termination)

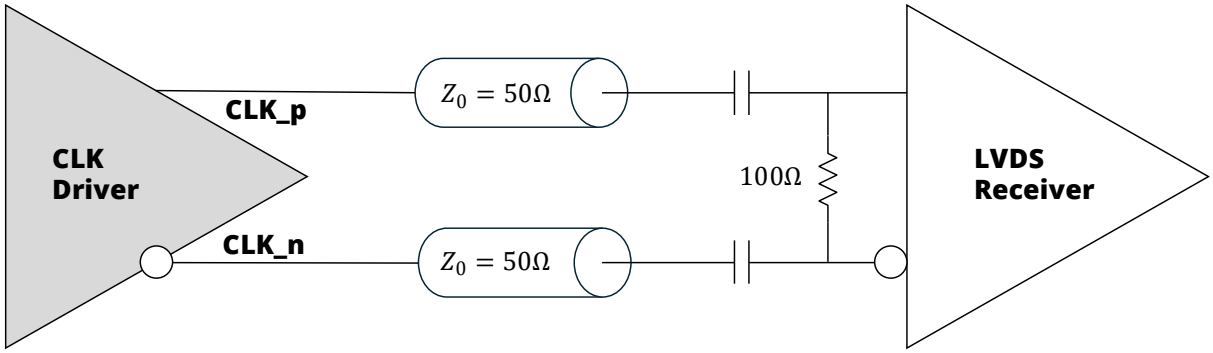


Figure 10. AC-Coupled LVDS

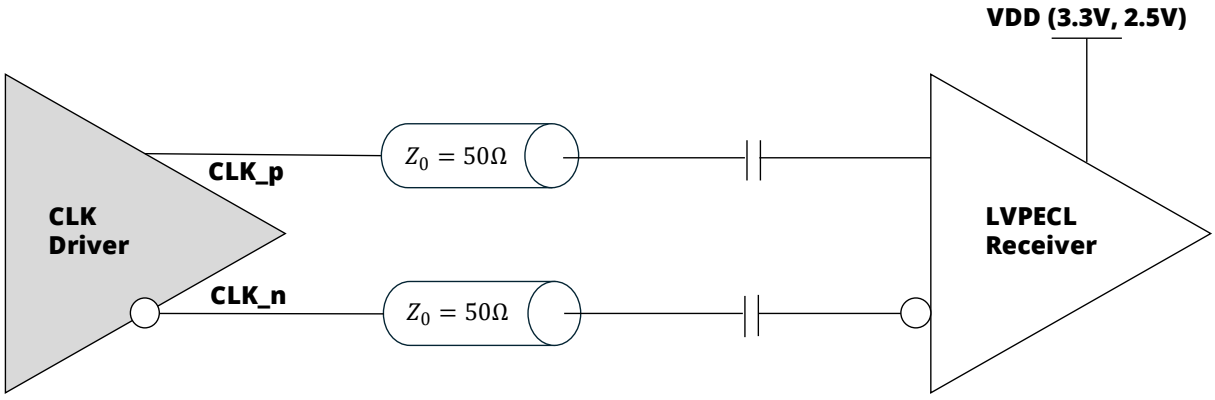


Figure 11. AC-Coupled LVPECL (Integrated Termination)

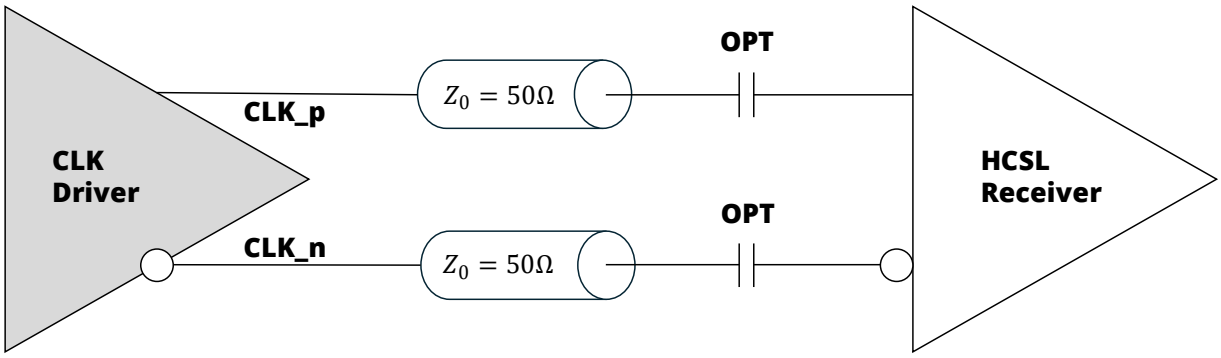


Figure 12. HCSL (Integrated Termination)

Packaging Information

Figure 13 shows the MS1220 packaging drawing.

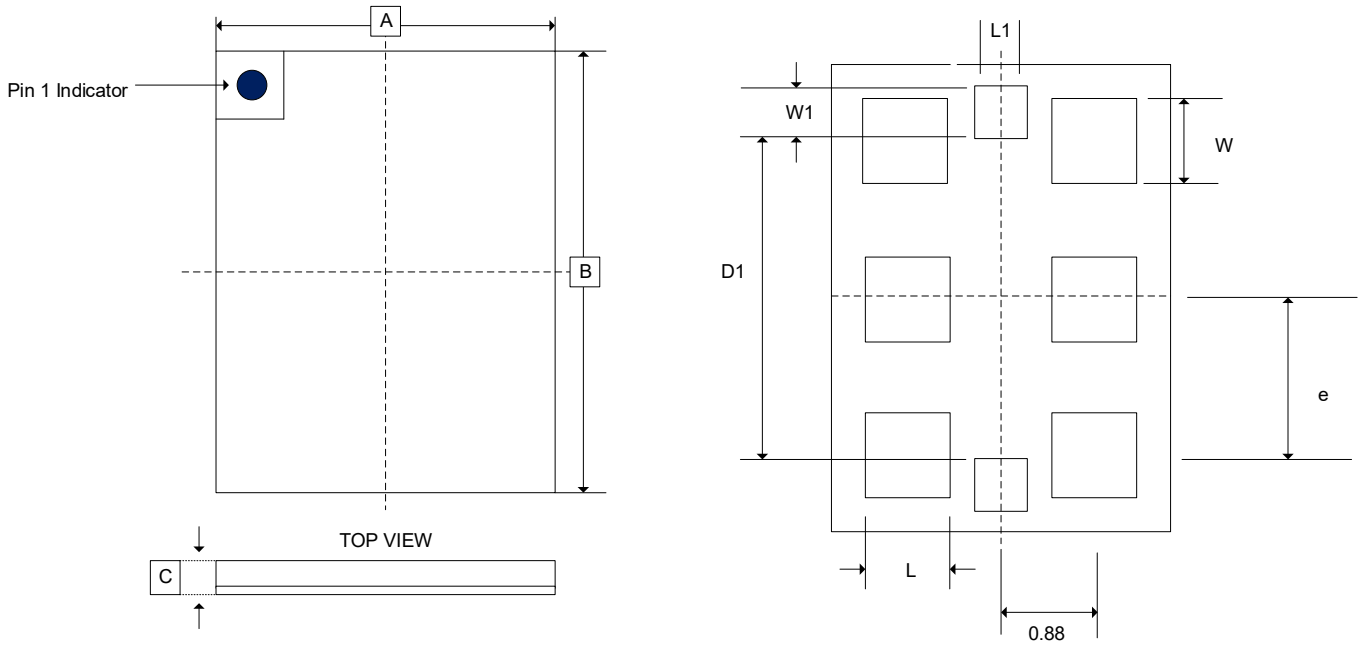


Figure 13. MS1220 Packaging Drawing (3.2mm x 2.5 mm)

Table 8. MS1220 Packaging Dimensions

Dimensions	Min	Nom	Max
A		2.5 BSC	
B		3.2 BSC	
C	0.806	0.946	1.1
W	0.55	0.6	0.65
L	0.5	0.55	0.6
W1	0.35	0.4	0.45
L1	0.35	0.4	0.45
e		1.1 BSC	
D1		2.2 BSC	
Package Edge Tolerance		0.1	
Mold Flatness		0.1	
Coplanarity		0.08	

Packaging Land Pattern

Figure 14 shows the MS1220 PCB land pattern.

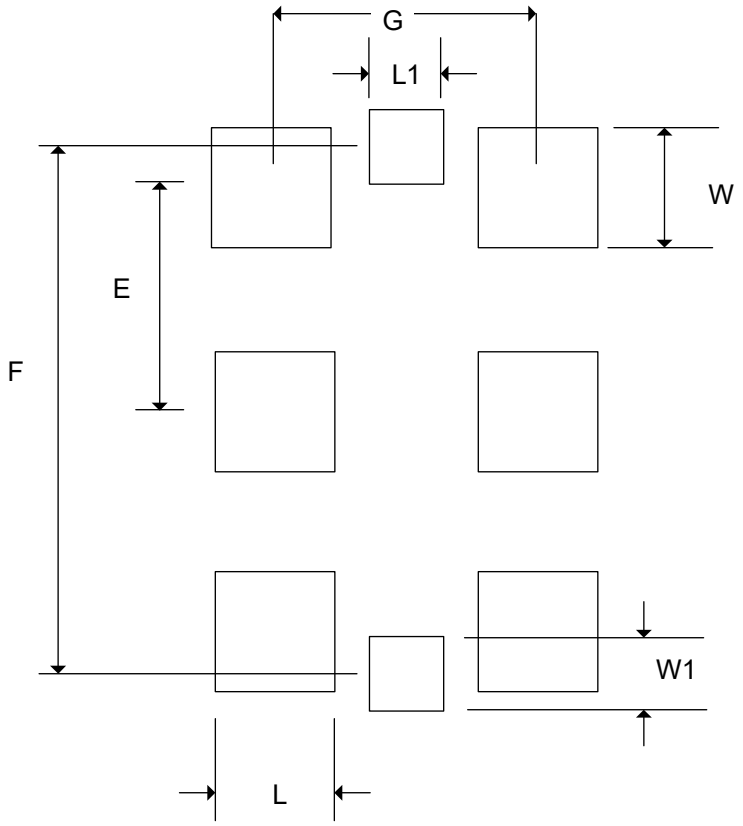


Figure 14. MS1220 Packaging Land Pattern Drawing (3.2mm x 2.5mm)

Table 9. MS1220 Packaging Land Pattern Dimensions

Dimensions	In mm
L	0.7
W	0.7
L1	0.5
W1	0.55
E	1.1
F	2.6
G	1.76

Device Top Marking

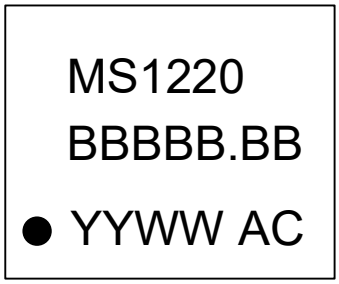


Figure 15. MS1220 Device Top Marking Showing Pin 1

Table 10. MS1220 Device Marking Legend

Line	Position	Description
1	1	Part Number
2	1-5	Wafer Lot Number
	6-7	Wafer #
3	Lot Traceability	
	1	Pin 1 Orientation Mark (Dot),
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	6-7	Assembly Code

Part Ordering Information

Figure 16 shows a logic tree for ordering each of the three available parts.

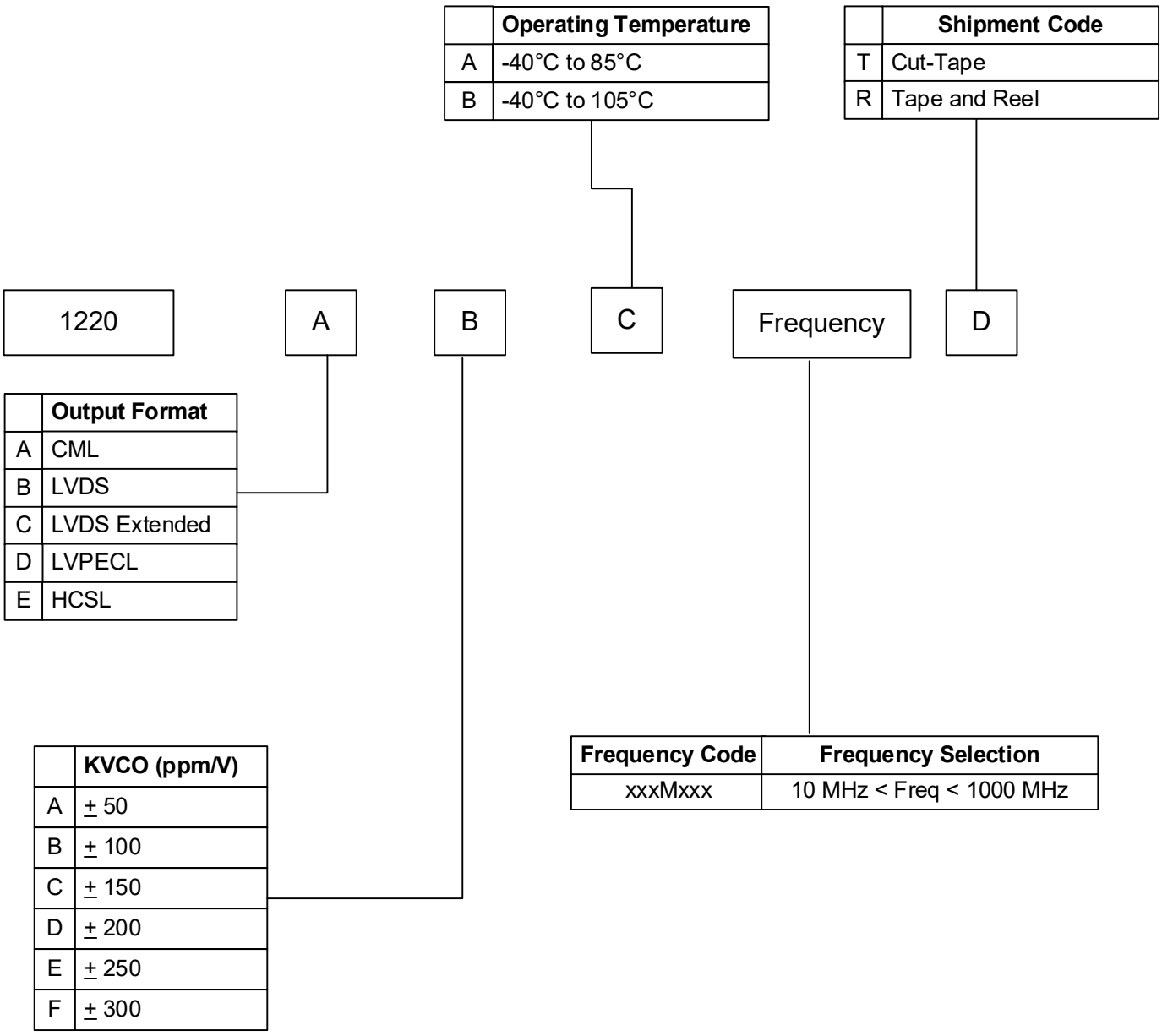


Figure 16. MS1220 Part Ordering Information

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