Ultra-Low Jitter Crystal Oscillators (XO)

Features

- Available at any frequency from 10 MHz to 1000 MHz
- Ultra-Low Jitter (12 KHz to 20 MHz)
  - 32 fs at 312.50 MHz
  - 34 fs at 491.52 MHz
- Total stability of ±20 ppm
- CML/LVDS/LVPECL/HCSL output formats
- Output Enable/Disable Feature
- < 10 ms start-up time
- No activity dips or micro jumps
- Industry standard 2.5X2.0 mm 6-pin LGA package
- Single 1.8V supply with internal regulator
- Superior power supply immunity
- Temperature range: -40°C to 85°C
- Temperature extended range: -40°C to 105°C
- ESD HBM 2000V, CDM 500V
- Lead free / RoHS compliant

Applications

- Network Equipment (Optical Modules, routers)
- 100G/200G/400G/800G OTN, Coherent optics
- Storage, switches, servers, NICs, accelerators
- Datacenter
- 3G to 24G SDI broadcast video
- 10G/40G/100G optical ethernet
- 56G/112G PAM4 Clocking
- Test and measurement equipment

General Description

The MS1130 is a crystal oscillator (XO) powered by our Virtual Crystal™ technology that enables very stable fully programmable multi-GHz clocks with extremely low phase noise.

Adaptive fully autonomous DSP algorithms running in the background continuously monitor and ensure robust and consistent performance over process, voltage and temperature variations.

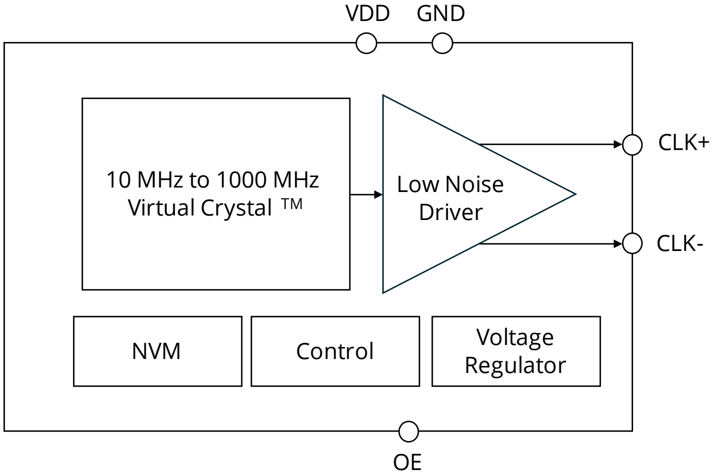
The devices are factory programmed to provide any frequency between 10 MHz and 1000 MHz with less than 1 ppb resolution.

The MS1130 is manufactured in a high-volume 28 nm CMOS process and represents the most advanced node in the timing industry.

Device Information

Part Number	Package	Description
MS1130	2.5x2.0 mm 6-pin LGA	Single frequency

Figure 1. Functional Block Diagram



MS1130

Single Frequency Device

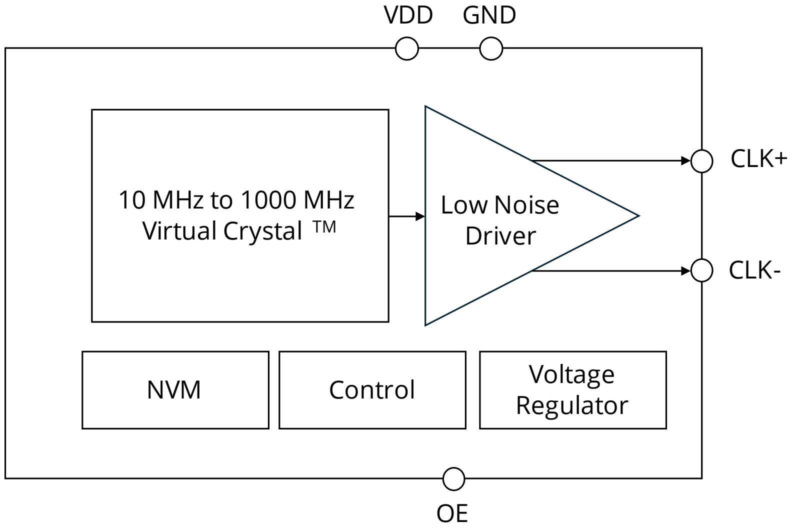


Figure 2. MS1130 Functional Block Diagram

Pin Assignment and Pin Description

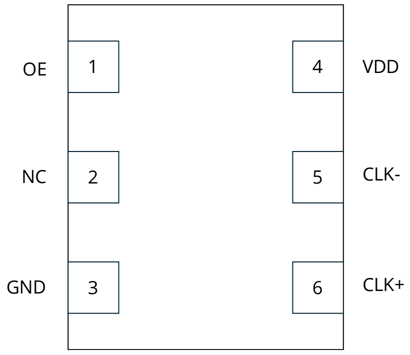


Figure 3. MS1130 Pin Assignments

Table 1. MS1130 Pin Descriptions

Pin No	Name	Description
1	OE	Output Enable
2	NC	No Connect
3	GND	Ground
4	CLK+	Clock Output
5	CLK-	Complementary Clock Output
6	VDD	Power Supply

Specifications

Table 2. Electrical Specifications

Typical values are specified at T_A= 25°C, V_{DD}=1.8V unless otherwise specified. All Min and Max limits are specified over the operating temperature range and voltage range with standard termination. A 0.1uF and 10uf bypass capacitor should be connected between VDD and GND pins located close to the device.

Parameter	Symbol	Test Condition/Comment	Min	Typ	Max	Unit

Frequency Range

Frequency Range	F_{CLK}	All Output Formats	10		1000	MHz

Frequency Stability

Frequency Stability*	F_{STB}	-40°C to 85°C	-20		20	PPM
Frequency Stability*	F_{STB}	-40°C to 105°C	-25		25	PPM
*Frequency stability includes initial tolerance, voltage tolerance, operating temperature and aging (10 year, +25°C). Aging is estimated from environmental reliability tests;						

Clock Output Jitter Characteristics

RMS Phase Jitter (12 KHz – 20 MHz)	Φ_{JITTER}	Frequency=312.5 MHz		32		fs
Note: Phase jitter measured on Agilent 5052B Signal Source Analyzer						

Operating Voltage/Temperature Range

Supply Voltage	V_{DD}		1.71	1.8	1.89	V
Temperature Range	T_A	Industrial Temperature	-40		85	°C
		Extended Industrial Temperature	-40		105	°C

Current Consumption

Supply Current	I_{DD}	LVDS Output (Output Enabled)		80	100	mA
		All Other Outputs (Output Enabled)		90	110	mA
		Tristate Hi-Z (Output Disabled)		50	60	mA

Input Characteristics

Digital Input Levels (OE)	V_{IH}		$0.7XV_{DD}$			V
	V_{IL}				$0.3XV_{DD}$	V
Output Enable (OE)	T_D	Output Disable Time			3	us
	T_E	Output Enable Time			20	us
Powerup Time	T_{PWR}	Time from 0.9xVDD until output frequency (F_{CLK}) within spec			10	ms

PSRR Characteristics

PSRR	$PSRR_{SPUR}$	Spurs induced by 50mV power supply ripples (All frequency, all output types)		-100		dBc

Note:

(1) Measured maximum spur level with 50mVpp sinusoidal signal between 50 kHz and 1 MHz applied on VDD Pin

Output Characteristics

Output Duty Cycle	DC	All Output Formats	48		52	%
Output Rise/Fall Time (20% to 80% V_{PP})	T_R / T_F	All Output Formats		65	100	ps
LVDS Output (AC Mode)	V_O	Swing (Diff)	0.5	0.7	0.9	V
LVDS Extended Output (AC Mode)	V_O	Swing (Diff)	0.8	1.2	1.6	V
CML Output (AC Mode)	V_O	Swing (Diff)	0.7	0.85	1	V
LVPECL Output (AC Mode) Integrated Termination	V_O	Swing (Diff)	1.2	1.4	1.6	V
HCSL Output Integrated Termination	V_O	Swing (Diff)	1.2	1.4	1.6	V

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Unit
1.8V Supply Voltage	-0.3	1.98	V
Digital I/O	-0.3	1.98	V
Maximum Operating Temperature		105	°C
Storage Temperature	-55	150	°C
Soldering Temperature		260	°C
Junction Temperature		150	°C
Note: Stresses that exceed what is listed in this table may cause permanent damage to the device. Exposure to conditions above the recommendations for extended periods of time may affect device reliability.			

Table 4. Environmental Compliance

Parameter	Test Condition
Mechanical Shock	MIL-STD-883, Method 2002
Mechanical Vibration	MIL-STD-883, Method 2007
Moisture Sensitivity Level (MSL)	3
Note: For additional information not listed, please contact Mixed-Signal Devices.	

Table 5. ESD Levels

Description	Description	Specification	Level
HBM[1]	Human Body Model	JEDEC JS-001	2000V
CDM[2]	Charge Device Model	JEDEC JESD22-C101	500V
Notes: 1. 1000V HBM allows safe manufacturing with standard ESD control process – JEDEC document JEP155 2. 250V CDM allows safe manufacturing with standard ESD control process – JEDEC document JEP157			

Table 6. Package Thermal Information

Package	Parameter	Symbol	Value	Unit
2.5mm x 2mm 6 pin LGA	Thermal Resistance, Junction to Ambient	$ø_{JA}$	90	°C/W
	Thermal Resistance, Junction to Board	$ø_{JB}$	40	°C/W
	Air Flow Condition		0	mps
	Maximum Junction Temperature	T_J	125	°C
Note: The thermal resistance information stated in this table is based on a standard JEDEC PCB condition. The actual thermal resistance varies depending on the customer PCB design.				

Table 7. Typical Output Phase Noise Characteristics

VDD= 1.8V, T_A = 25°C, Output Type = CML

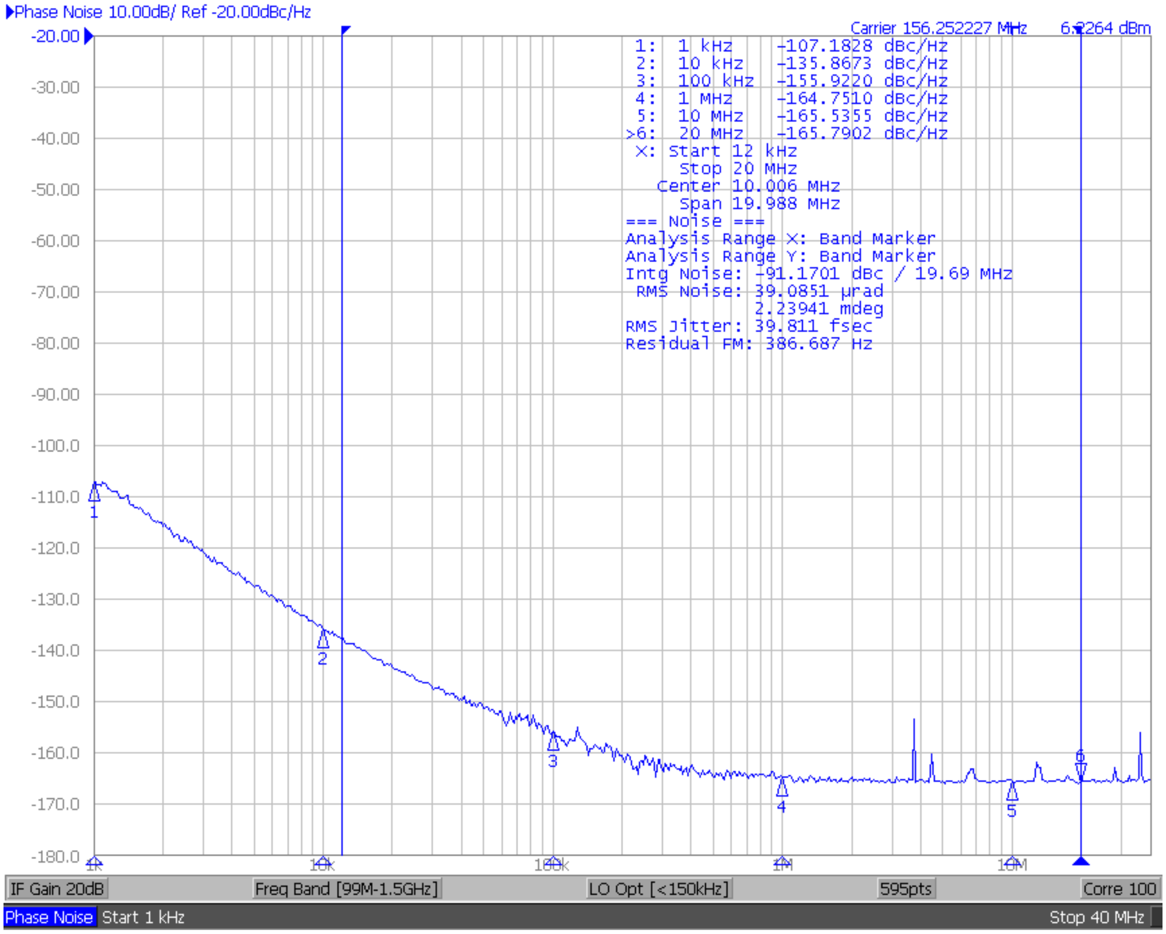
Offset frequency	156.25 MHz	312.50 MHz	491.52 MHz	625.00 MHz	Unit
1 KHz	-107	-101	-96	-94	dBc/Hz
10 KHz	-136	-130	-126	-124	dBc/Hz
100 KHz	-156	-152	-148	-145	dBc/Hz
1 MHz	-165	-161	-156	-153	dBc/Hz
10 MHz	-166	-162	-157	-154	dBc/Hz
20 MHz	-166	-162	-157	-154	dBc/Hz
RMS Jitter (12 KHz – 20 MHz)	39.8 fs	31.9 fs	34.3 fs	38.2 fs	fs

Typical Output Measured Phase Noise Plots

This section shows MS1130 performance plots.

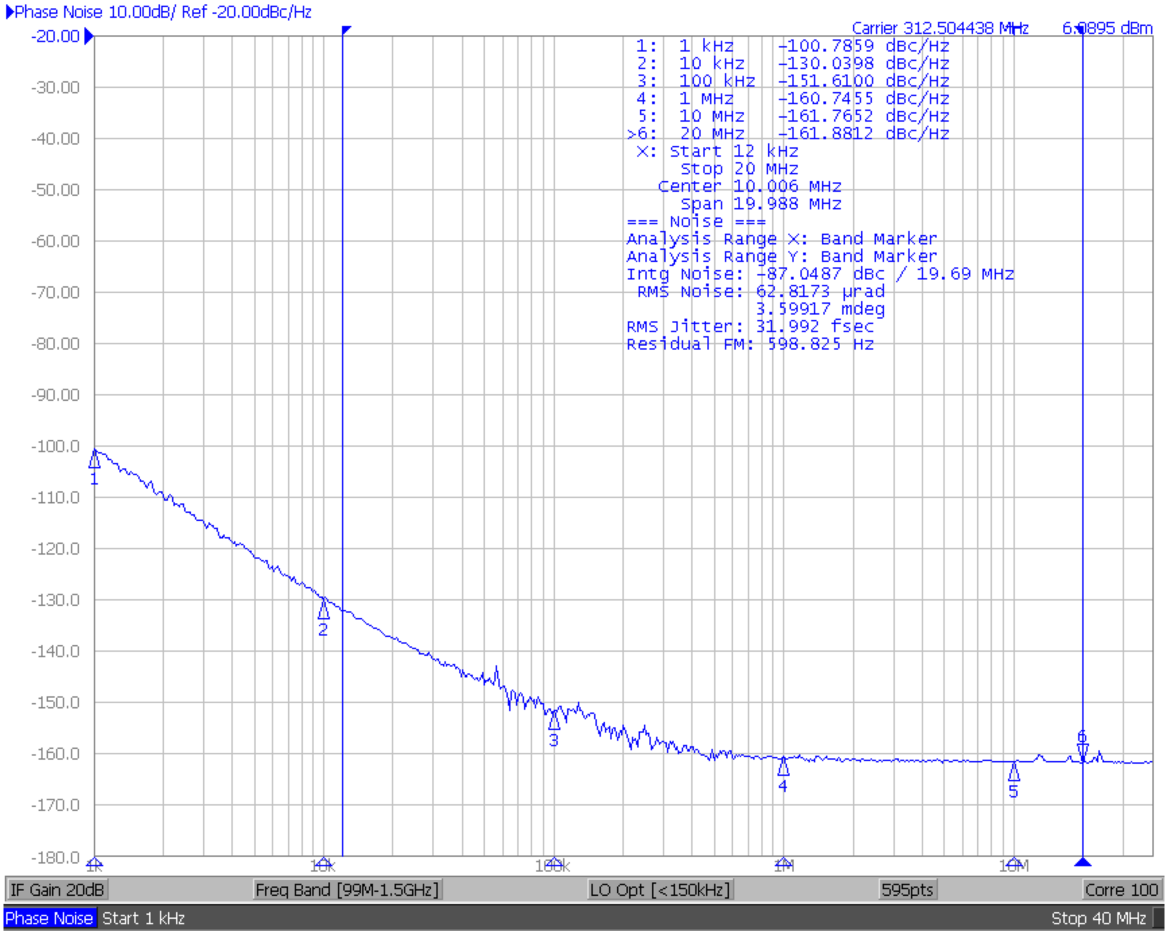
Measurement parameters are: VDD = 1.8 V, TA = 25°C, Output Type = CML.

The plots were captured using an Agilent E5052B Signal Source Analyzer.



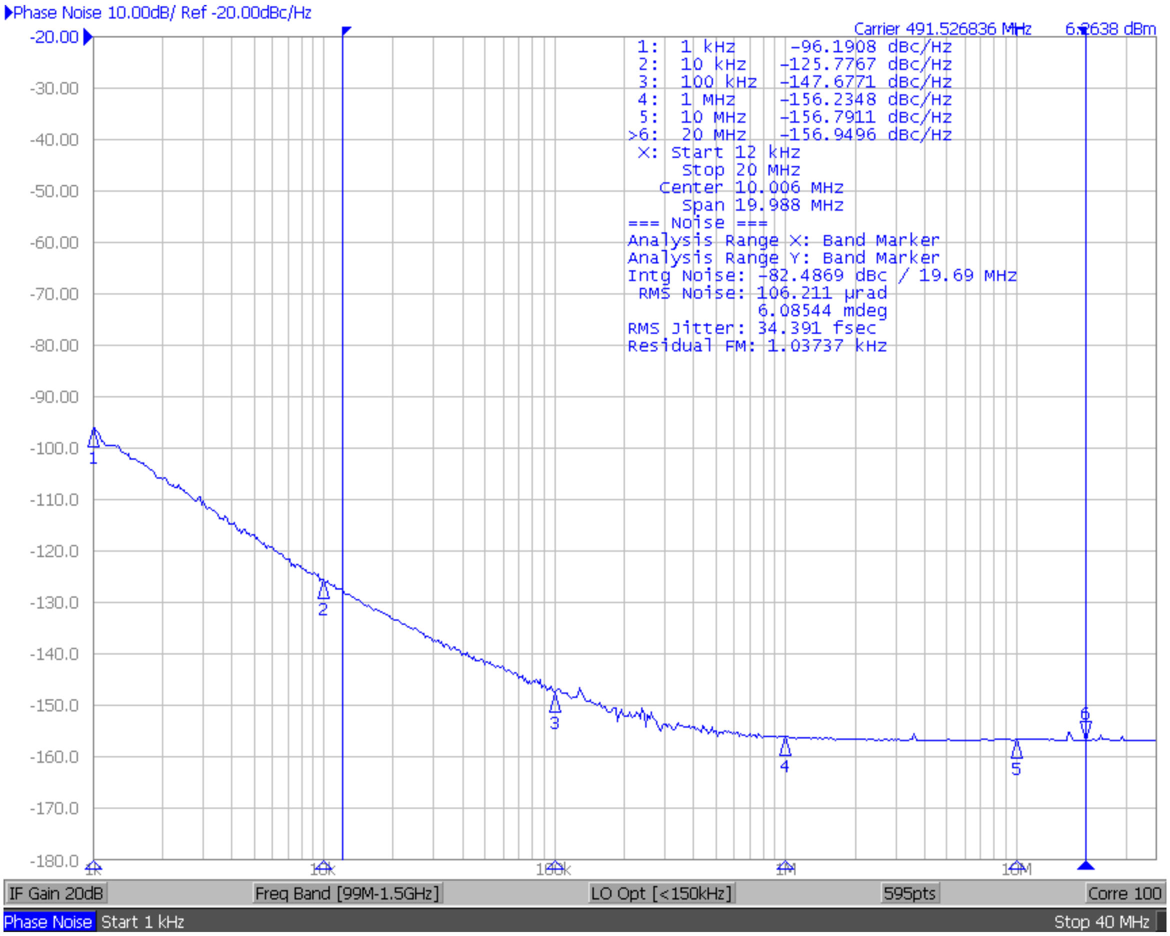
```
Carrier 156.252227 MHz      6.2264 dBm
 1:   1 kHz     -107.1828 dBc/Hz
 2:   10 kHz    -135.8673 dBc/Hz
 3:   100 kHz   -155.9220 dBc/Hz
 4:   1 MHz     -164.7510 dBc/Hz
 5:   10 MHz    -165.5355 dBc/Hz
>6:   20 MHz    -165.7902 dBc/Hz
 X: Start 12 kHz
      Stop 20 MHz
    Center 10.006 MHz
      Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -91.1701 dBc / 19.69 MHz
 RMS Noise: 39.0851 µrad
            2.23941 mdeg
RMS Jitter: 39.811 fsec
Residual FM: 386.687 Hz
```

Figure 4. Carrier: 156.25 MHz



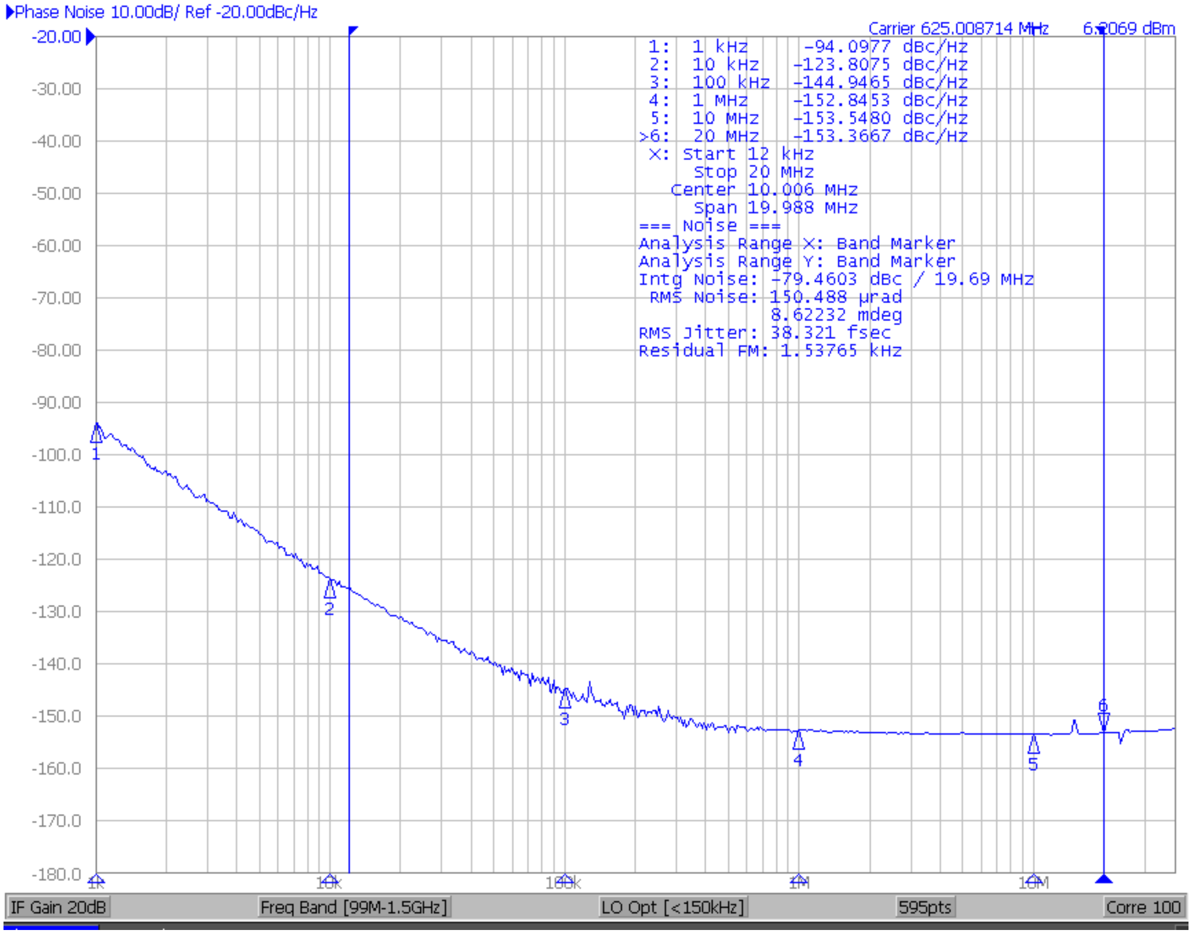
```
 1:  1 kHz      -100.7859 dBc/Hz
 2:  10 kHz     -130.0398 dBc/Hz
 3:  100 kHz    -151.6100 dBc/Hz
 4:  1 MHz      -160.7455 dBc/Hz
 5:  10 MHz     -161.7652 dBc/Hz
>6:  20 MHz     -161.8812 dBc/Hz
 X: Start 12 kHz
        Stop 20 MHz
      Center 10.006 MHz
        Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -87.0487 dBc / 19.69 MHz
 RMS Noise: 62.8173 µrad
            3.59917 mdeg
RMS Jitter: 31.992 fsec
Residual FM: 598.825 Hz
```

Figure 5. Carrier: 312.5 MHz



```
 1:  1 kHz       -96.1908 dBc/Hz
 2:  10 kHz    -125.7767 dBc/Hz
 3:  100 kHz   -147.6771 dBc/Hz
 4:  1 MHz     -156.2348 dBc/Hz
 5:  10 MHz    -156.7911 dBc/Hz
>6:  20 MHz    -156.9496 dBc/Hz
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -82.4869 dBc / 19.69 MHz
 RMS Noise: 106.211 µrad
            6.08544 mdeg
RMS Jitter: 34.391 fsec
Residual FM: 1.03737 kHz
```

Figure 6. Carrier: 491.52 MHz



```
 1:  1 kHz      -94.0977 dBc/Hz
 2:  10 kHz    -123.8075 dBc/Hz
 3:  100 kHz   -144.9465 dBc/Hz
 4:  1 MHz     -152.8453 dBc/Hz
 5:  10 MHz    -153.5480 dBc/Hz
>6:  20 MHz    -153.3667 dBc/Hz
 X: Start 12 kHz
     Stop 20 MHz
   Center 10.006 MHz
     Span 19.988 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -79.4603 dBc / 19.69 MHz
 RMS Noise: 150.488 µrad
            8.62232 mdeg
RMS Jitter: 38.321 fsec
Residual FM: 1.53765 kHz
```

Figure 7. Carrier: 625 MHz

Output Terminations

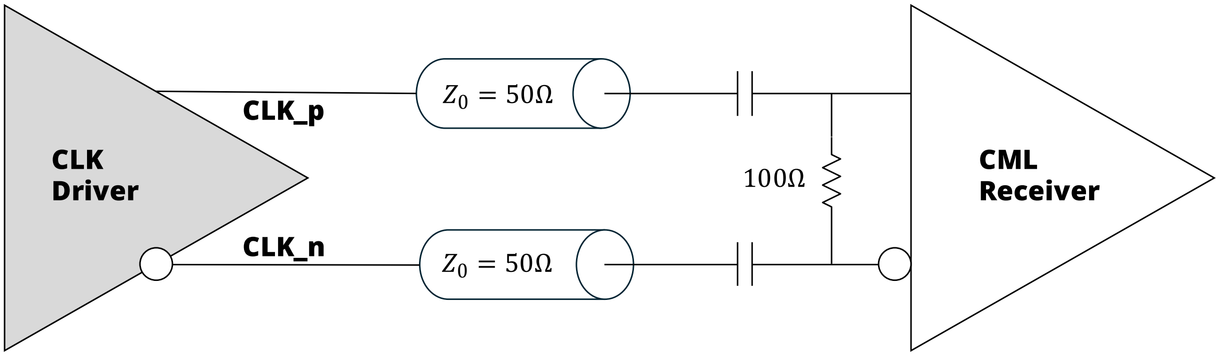


Figure 8. AC-Coupled CML

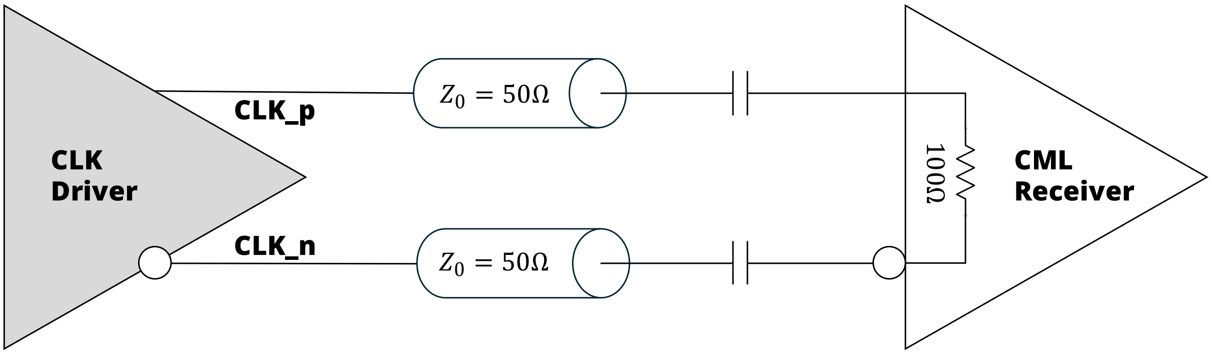


Figure 9. AC-Coupled CML (Receiver Termination)

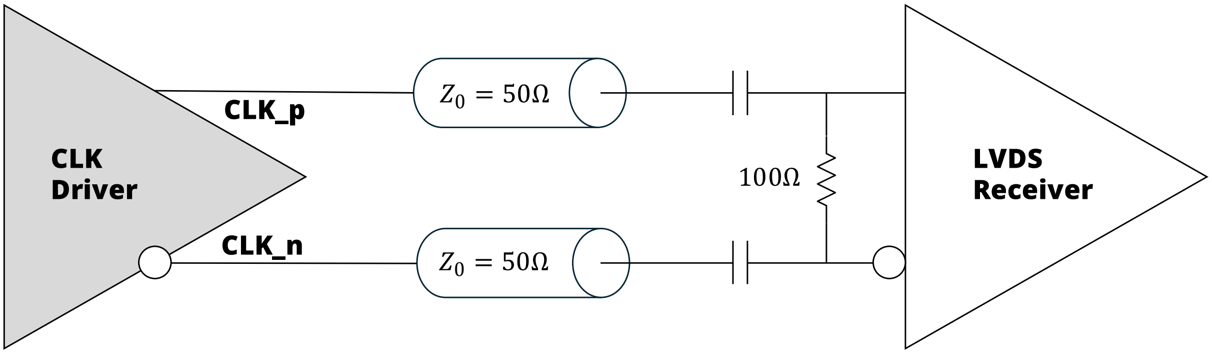


Figure 10. AC-Coupled LVDS

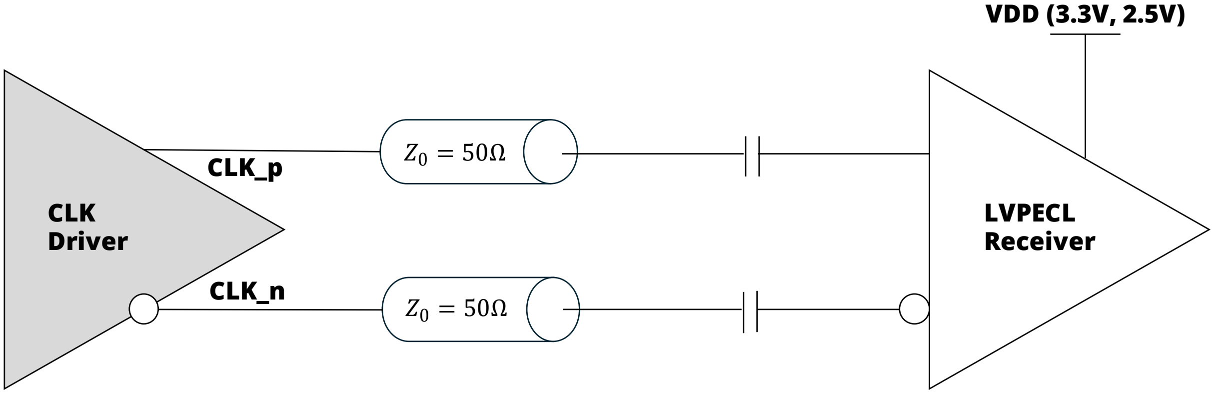


Figure 11. AC-Coupled LVPECL (Integrated Termination)

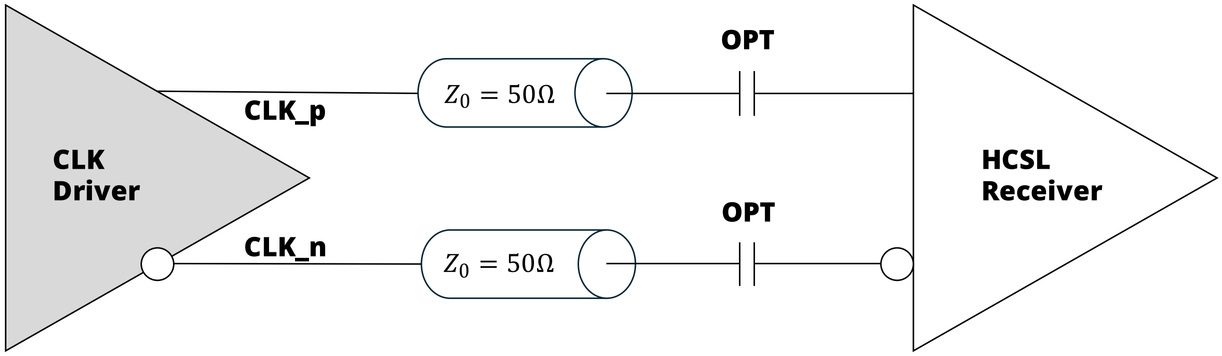


Figure 12. HCSL (Integrated Termination)

Packaging Information

Figure 13 shows the MS1130 packaging drawing.

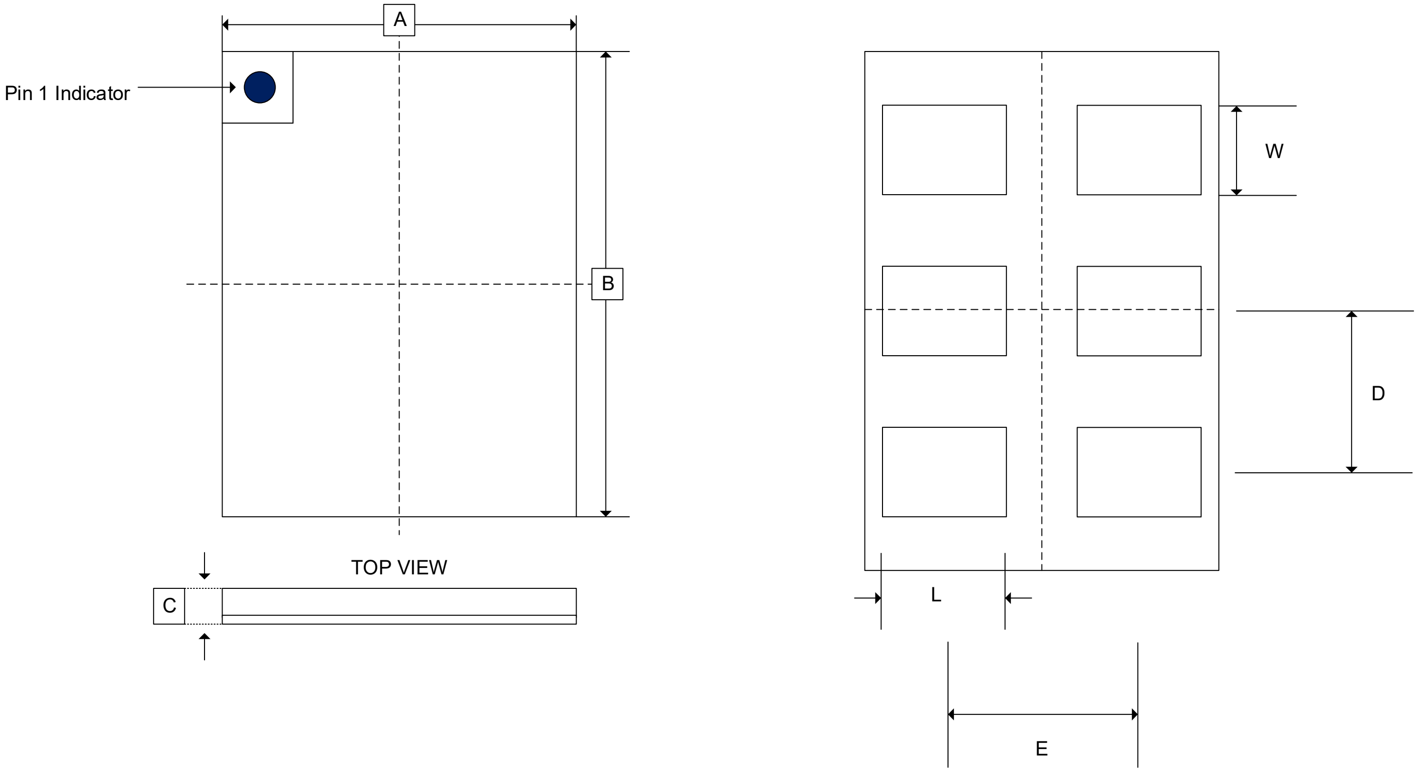


Figure 13. MS1130 Packaging Drawing (2.5X2.0 mm)

Table 8. MS1130 Packaging Dimensions

Dimensions	Min	Nom	Max
A	2.00 BSC		
B	2.50 BSC		
C	0.903	0.96	1.1
L	0.55	0.60	0.65
W	0.35	0.40	0.45
D	0.85 BSC		
E	1 BSC		
Package Edge Tolerance	0.1		
Mold Flatness	0.2		
Coplanarity	0.08		

Note: All dimensions are in millimeters

Packaging Land Pattern

Figure 14 shows the MS1130 PCB land pattern.

Note: All dimensions are in millimeters

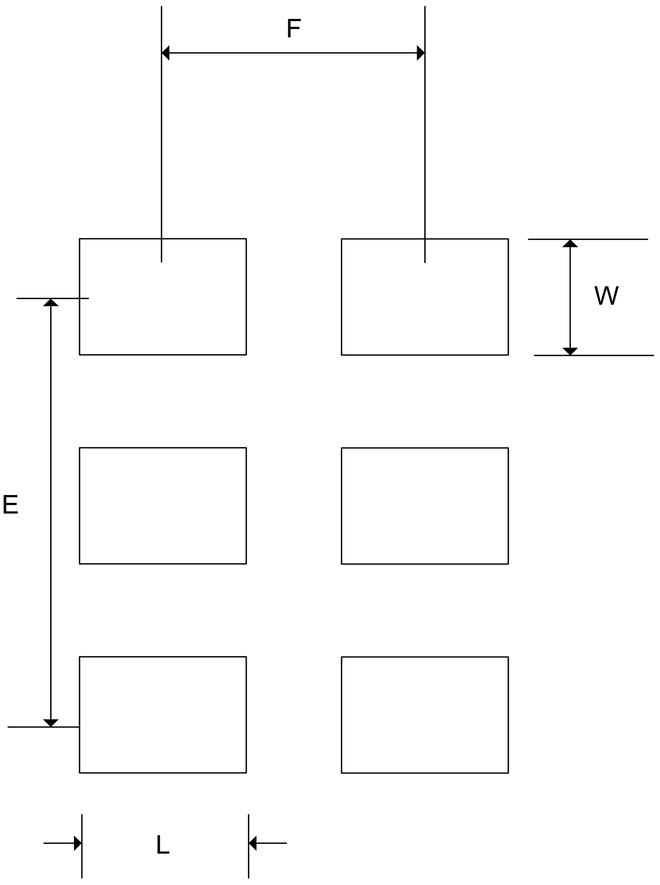


Figure 14. MS1130 Packaging Land Pattern Drawing (2.5X2.0 mm)

Table 9. MS1130 Packaging Land Pattern Dimensions

Dimensions	Length
L	0.75
W	0.55
E	1.7
F	1

Device Top Marking

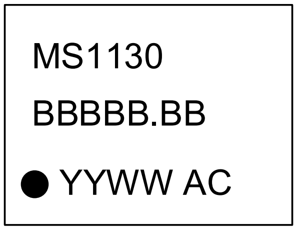


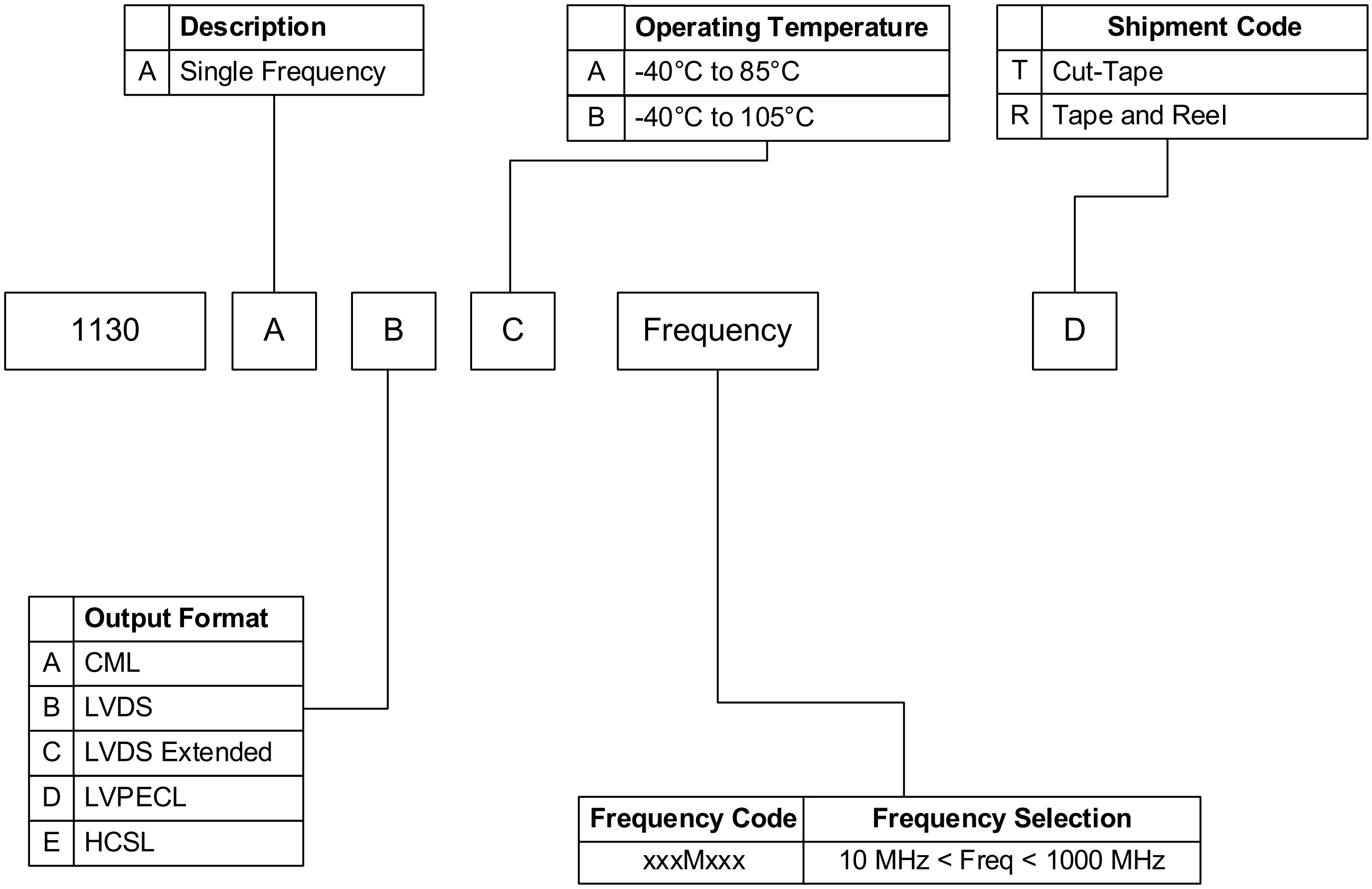
Figure 15. MS1130 Device Top Marking Showing Pin 1

Table 10. MS1130 Device Marking Legend

Line	Position	Description
1	1	Product Marking
2	1-5	Lot Number
	6-7	Wafer Number
3	Lot Trace Code	
	1	Pin 1 Orientation Mark (Dot)
	2-3	Year (last two digits of the year)
	4-5	Calendar Work Week Number (1-53)
	7-8	Assembly Code

Part Ordering Information

Figure 16 shows a logic tree for ordering each of the available parts.



	Description
A	Single Frequency

	Operating Temperature
A	-40°C to 85°C
B	-40°C to 105°C

	Shipment Code
T	Cut-Tape
R	Tape and Reel

	Output Format
A	CML
B	LVDS
C	LVDS Extended
D	LVPECL
E	HCSL

Frequency Code	Frequency Selection
xxxMxxx	10 MHz < Freq < 1000 MHz

Figure 16. MS1130 Part Ordering Information

IMPORTANT NOTICE AND DISCLAIMER

Mailing Address: Mixed-Signal Devices Inc, 2 Venture, Suite 300, Irvine, California 92618, USA